# Lenovo M910z Schematic Rev:1.0

RVP10


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| Reference | Description |
|---|---|
| CB | 0.1UF_0402 |
| CP | 0.01UF_0402 |
| CM | 1UF_0603 |

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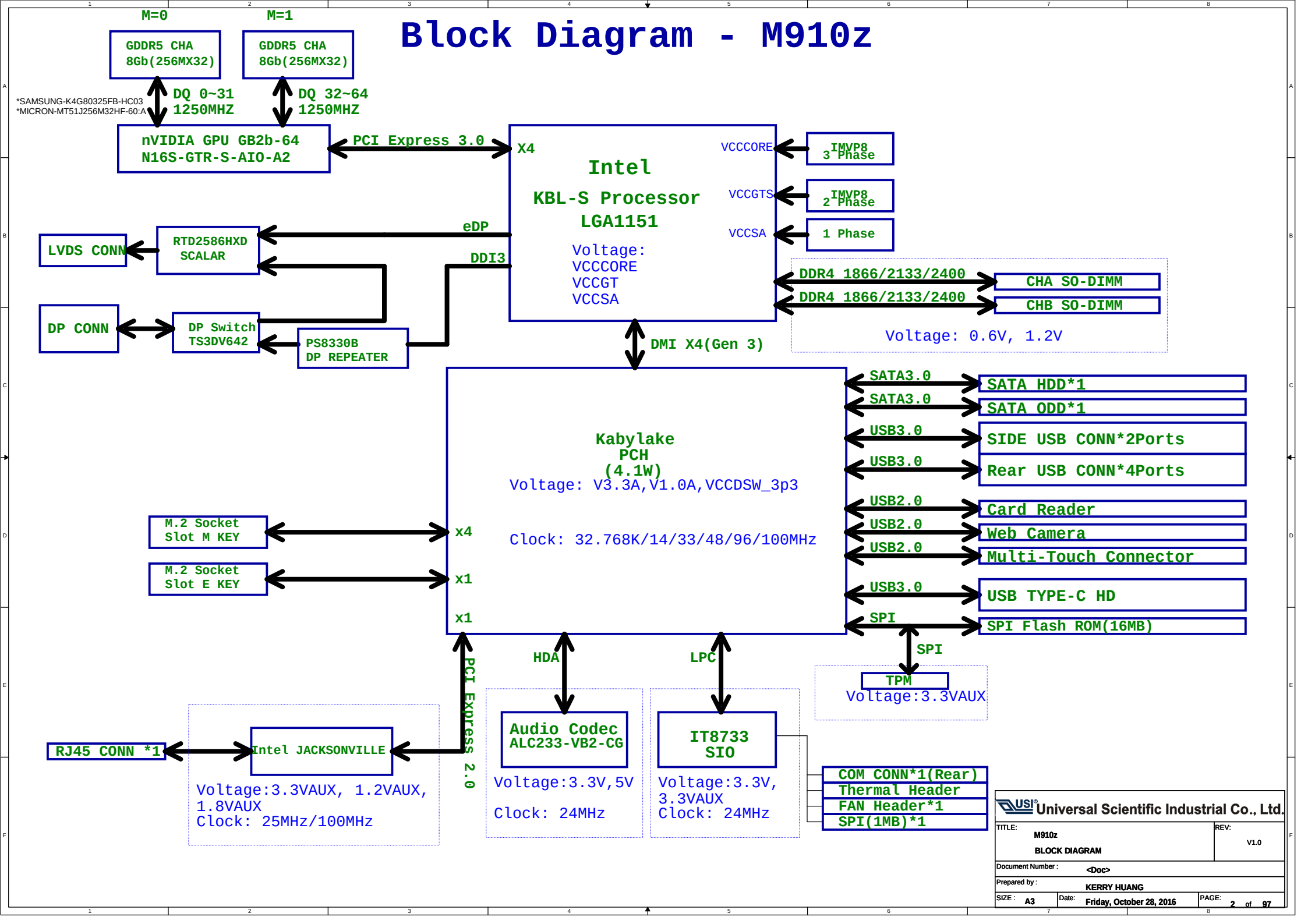
# Block Diagram - M910z

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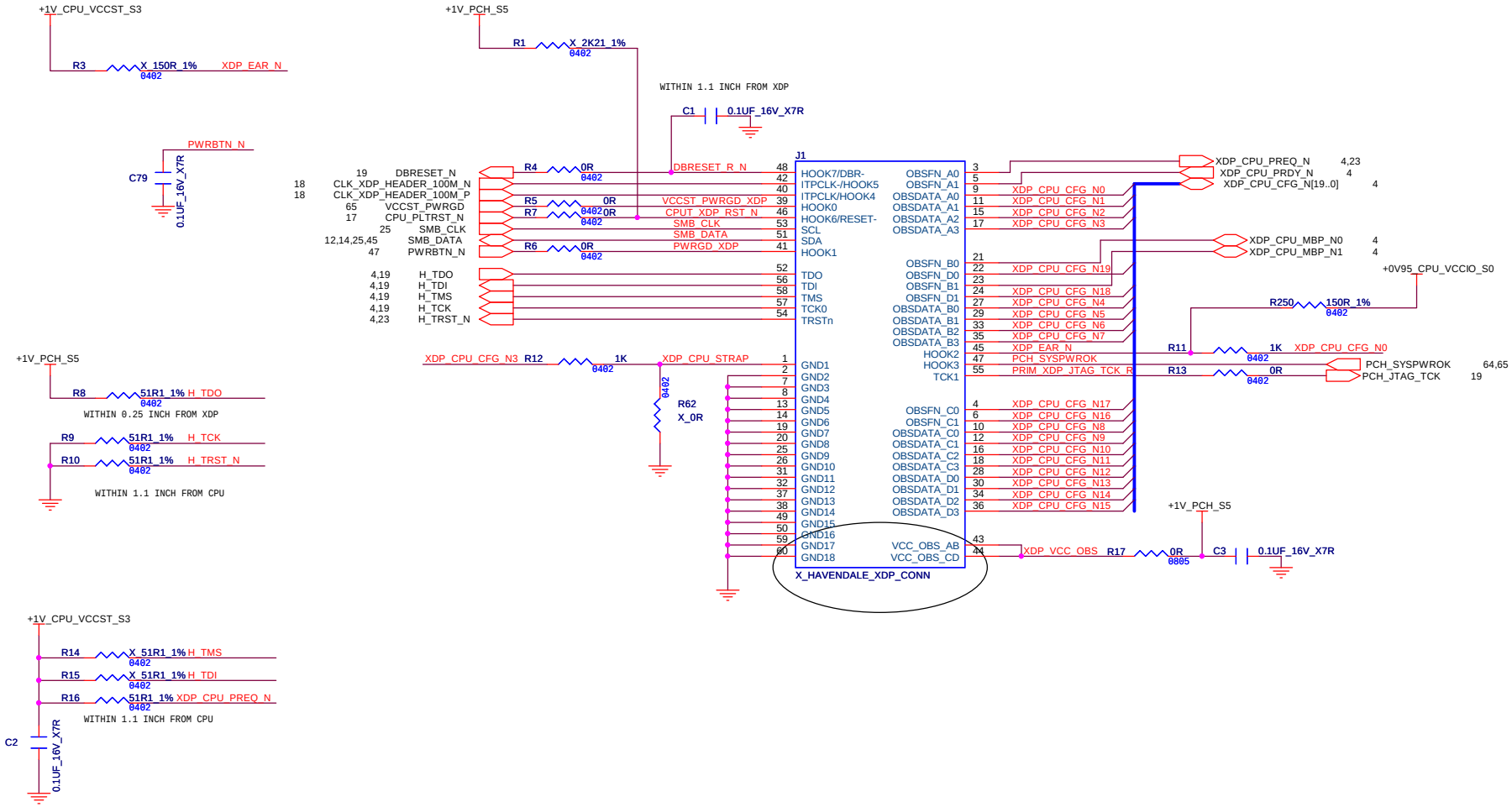
# CPU DEBUG CONN

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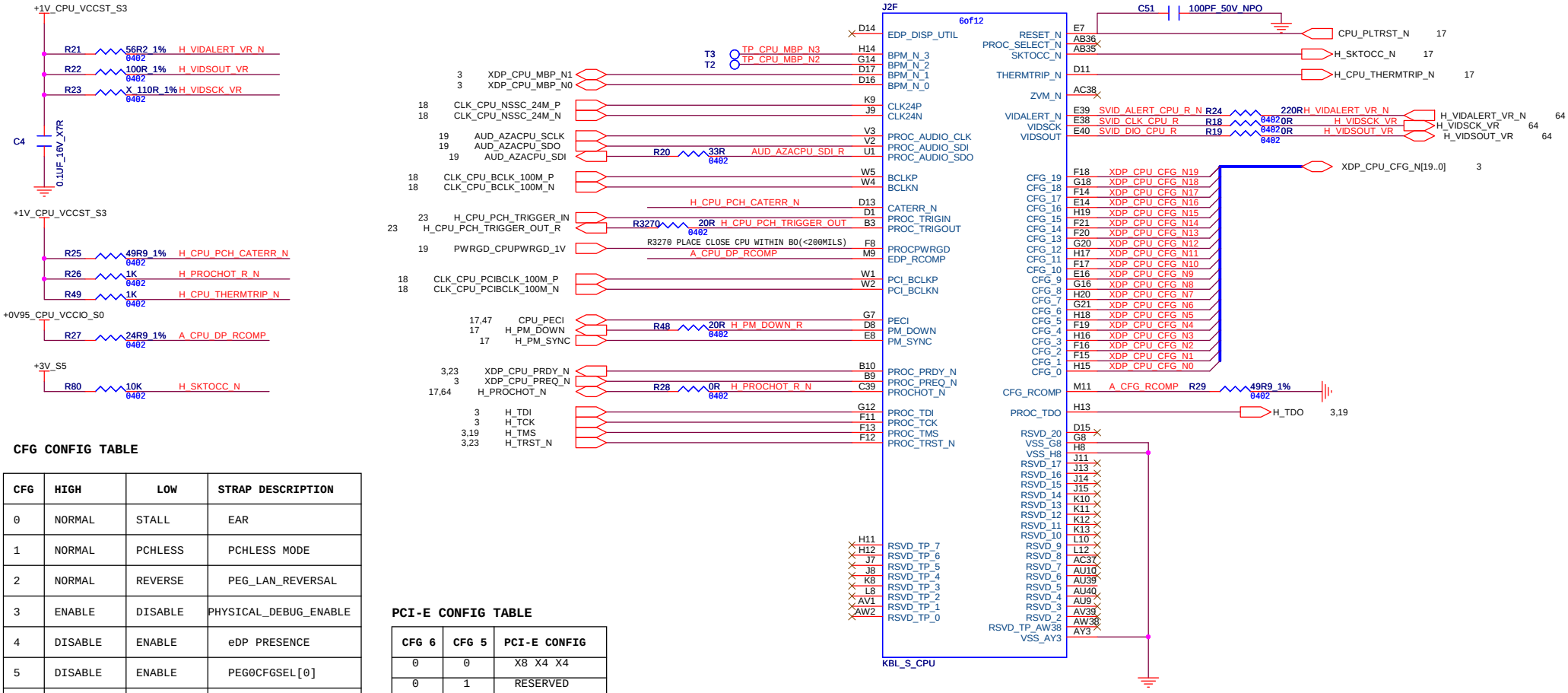
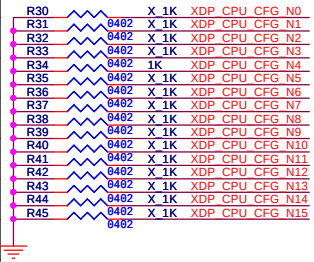



## CFG CONFIG TABLE

| CFG | HIGH | LOW | STRAP DESCRIPTION |
|---|---|---|---|
| 0 | NORMAL | STALL | EAR |
| 1 | NORMAL | PCHLESS | PCHLESS MODE |
| 2 | NORMAL | REVERSE | PEG_LAN_REVERSAL |
| 3 | ENABLE | DISABLE | PHYSICAL_DEBUG_ENABLE |
| 4 | DISABLE | ENABLE | eDP PRESENCE |
| 5 | DISABLE | ENABLE | PEG0CFGSEL[0] |
| 6 | DISABLE | ENABLE | PEG0CFGSEL[1] |
| 7 | RESET_N | BIOS REQ | PEG_DEFER_TRAINING |
| 8 | DISABLE | ENABLE | CFG UNLOCK |
| 9 | PRESENT | NOT PRESENT | SVID NOT PRESENT |
| 10 | ACTIVATE | DEACTIVATE | SAFE MODE BOOT |
| 11 | DC COUPLED | AC COUPLED | DMI_AC_COUPLED |
| 12 | PMSYNC 2.0 | LEGACY | PMSYNC LEGACY |
| 13 | SYNC | ASYNC | PMSYNC ASYNC MODE |
| 14 | RESERVE | | |
| 15 | RESERVE | | |
| ALL PINS HAVE INTERNAL PULL-UPS | | | |

## PCI-E CONFIG TABLE

| CFG 6 | CFG 5 | PCI-E CONFIG |
|---|---|---|
| 0 | 0 | X8 X4 X4 |
| 0 | 1 | RESERVED |
| 1 | 0 | X8 X8 |
| 1 | 1 | X16 |

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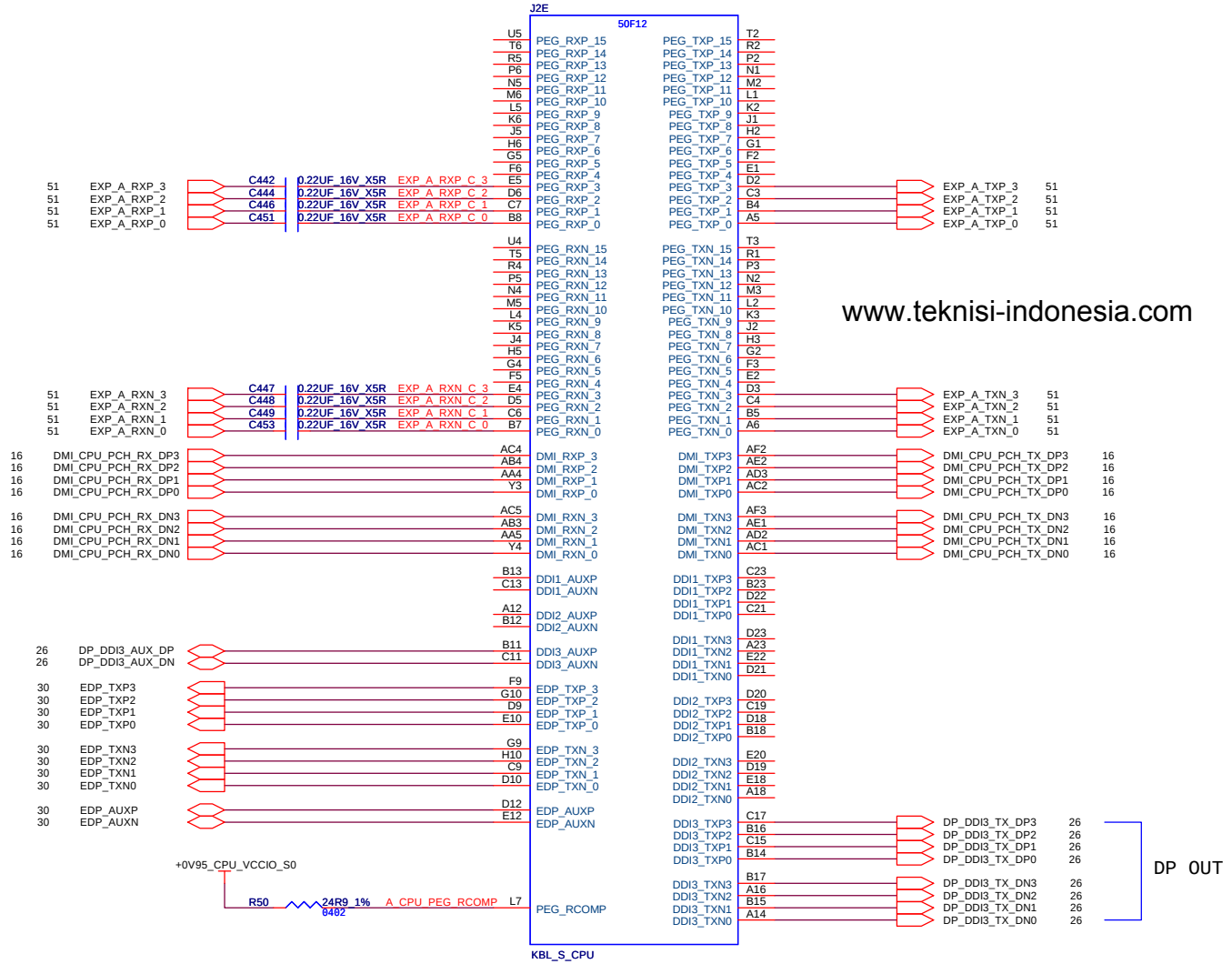


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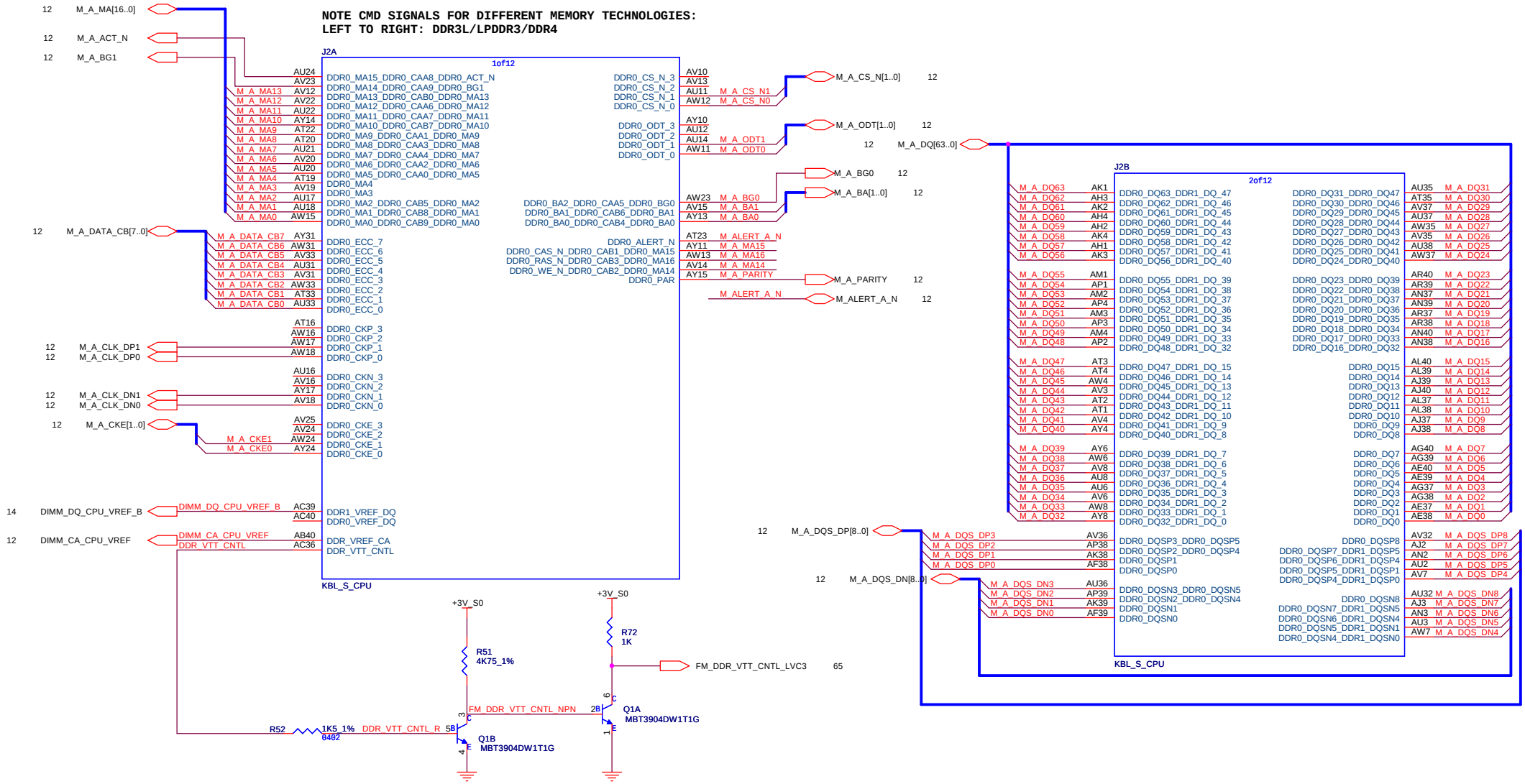
**NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHNOLOGIES:**
**LEFT TO RIGHT: DDR3L/LPDDR3/DDR4**

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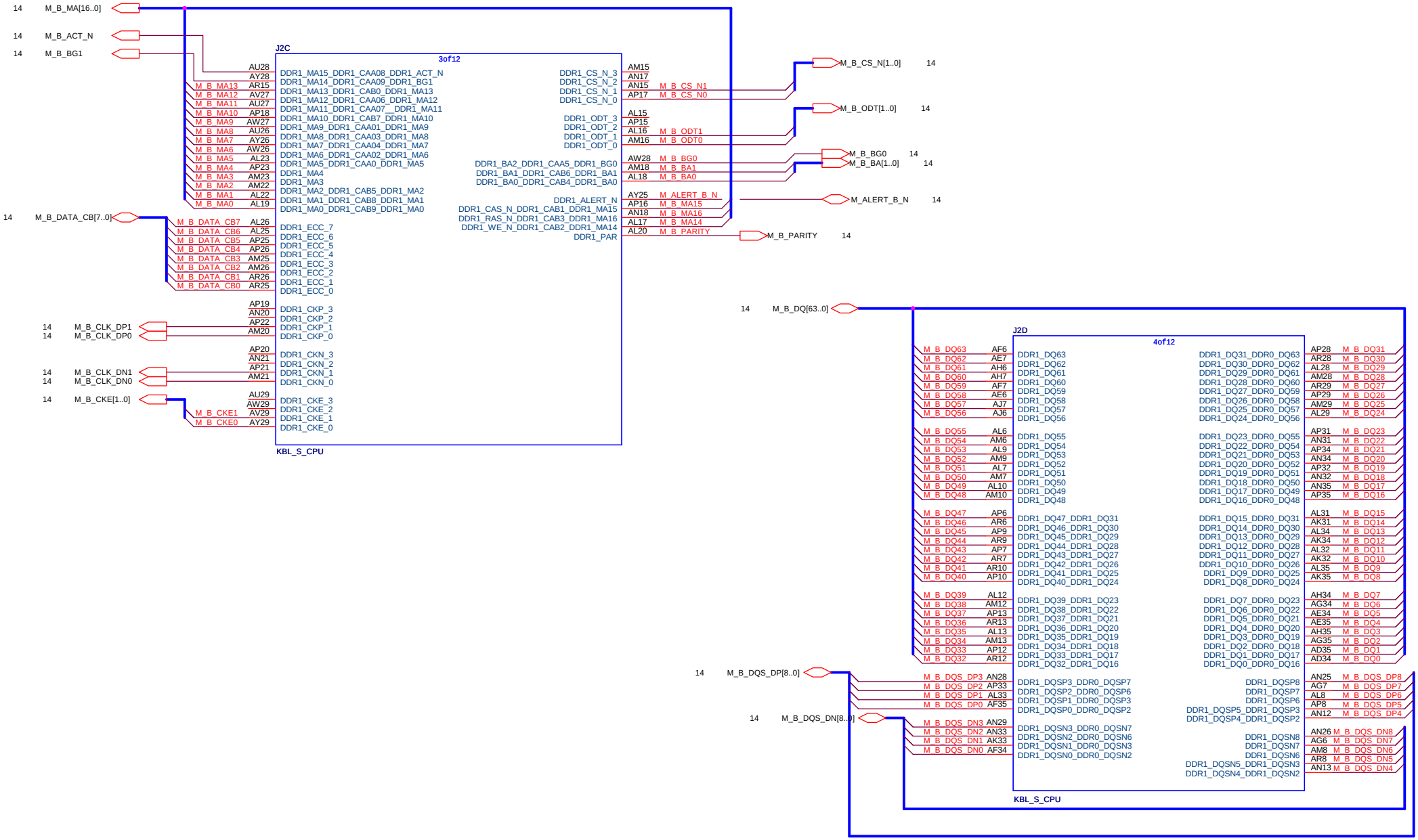
NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHNOLOGIES:
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4

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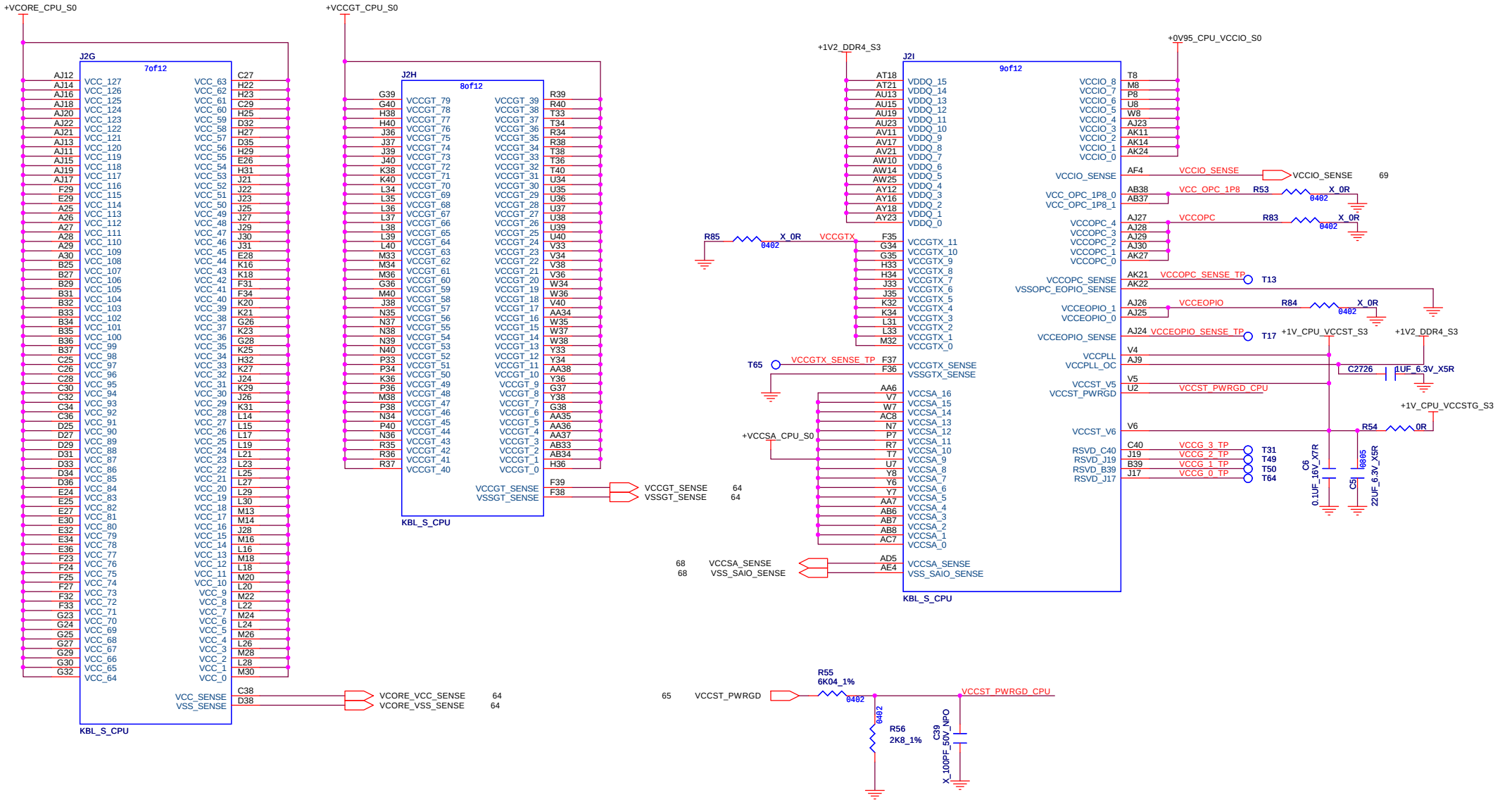


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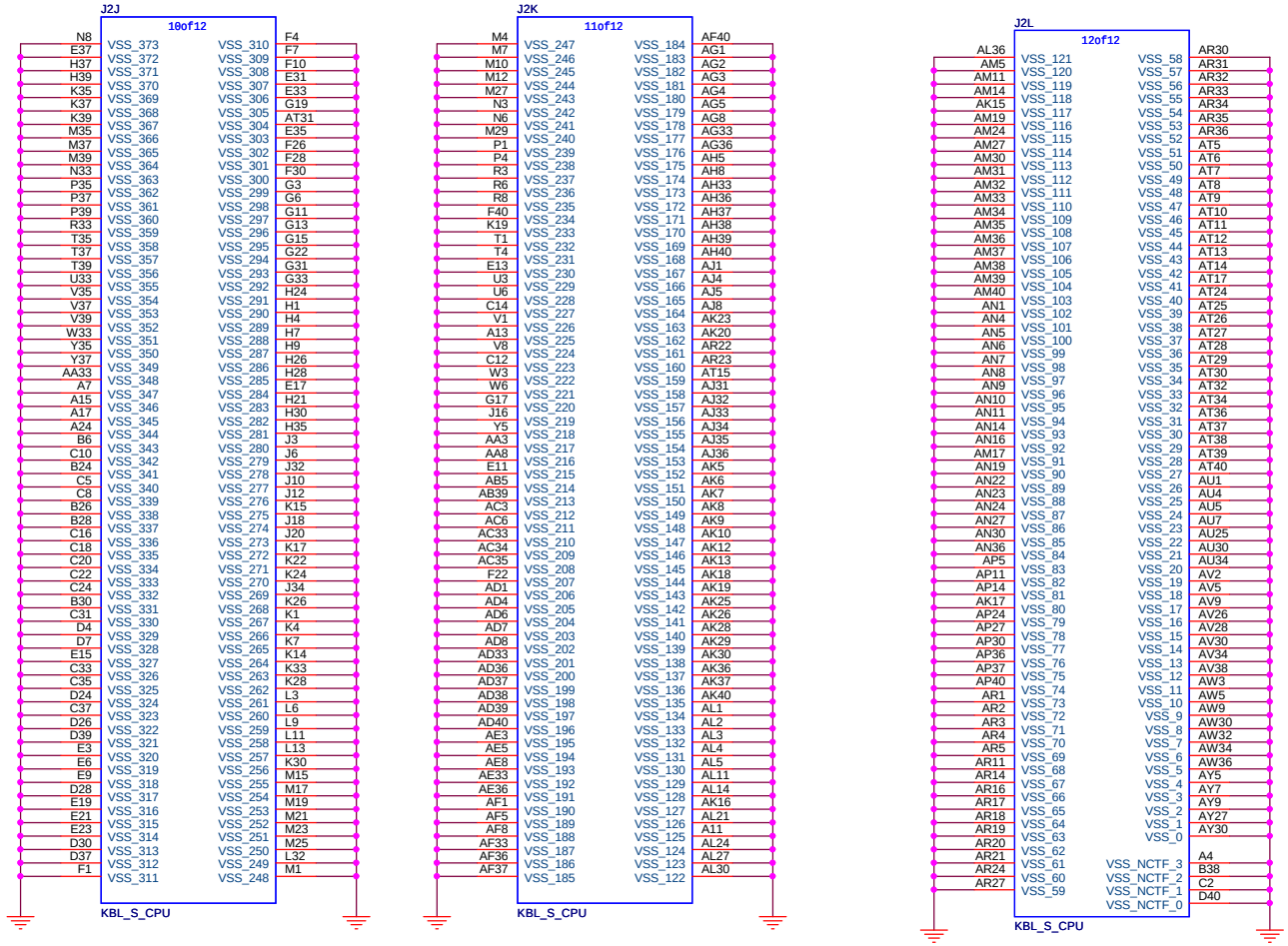


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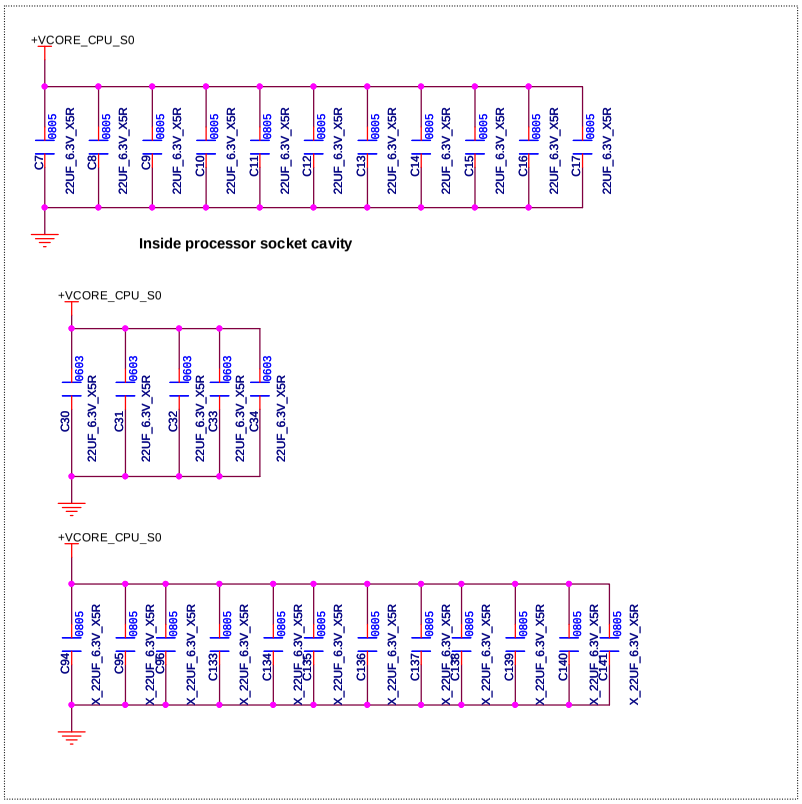
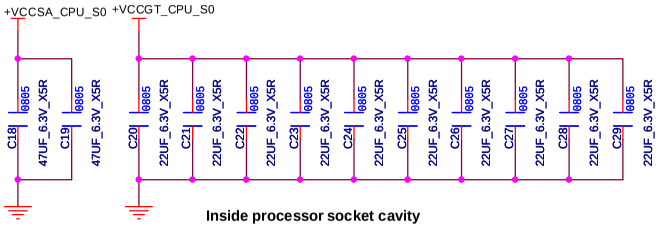
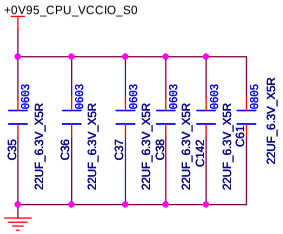
# CPU DECOUPLING

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# DDR4 SO-DIMM CHANNEL A

**CHANNEL A**
**ADDRESS:0XA0 000**

## DIMM1

CAD Note:
all signal should have
10 mil trace width

M_A_DQS_DP8 6
M_A_DQS_DN8 6
M_A_DQS_DP7 6
M_A_DQS_DN7 6
M_A_DQS_DP6 6
M_A_DQS_DN6 6
M_A_DQS_DP5 6
M_A_DQS_DN5 6
M_A_DQS_DP4 6
M_A_DQS_DN4 6
M_A_DQS_DP3 6
M_A_DQS_DN3 6
M_A_DQS_DP2 6
M_A_DQS_DN2 6
M_A_DQS_DP1 6
M_A_DQS_DN1 6
M_A_DQS_DP0 6
M_A_DQS_DN0 6
M_A_ODT1 6
M_A_ODT0 6

+1V2_DDR4_S3
R57 240R_1% 0402
M_A_TS_EVENT_N
6 M_A_DATA_CB[7..0]
M_A_DATA_CB0
M_A_DATA_CB1
M_A_DATA_CB2
M_A_DATA_CB3
M_A_DATA_CB4
M_A_DATA_CB5
M_A_DATA_CB6
M_A_DATA_CB7

M_A_DQ[63..0] 6

J3A
1of2
DDR4SODIMM260_RVS_ADDR0068P005A BLACK

+1V2_DDR4_S3
+3V_S0
R58 0R
CB1

M_A_PARITY 6
M_A_ALERT_A_N 6
M_A_ACT_N 6
M_A_BG0 6
M_A_BG1 6
M_A_CLK_DP0 6
M_A_CLK_DN0 6
M_A_CLK_DP1 6
M_A_CLK_DN1 6
M_RESET_N 14,19
M_A_CS_N[1..0] 6
M_A_CKE[1..0] 6
M_A_BA[1..0] 6
SMB_DATA 3,14,25,45
SMB_CLK 25

M_A_MA[16..0] 6

CAD NOTE:
PLACE RESISTORS
CLOSE TO CH_A DIMMS
ON DIMM_VREF_A

+1V2_DDR4_S3
R59 1K_1%
R63 1K_1%
C2724 1UF_6.3V_X5R

6 DIMM_CA_CPU_VREF
R65 2R_1% 0402
DIMM_CA_VREF_A
C40 0.022UF_25V_X7R
DIMM_CA_CPU_VREF_RC_A
R67 24R9_1%
C2175 4.7UF_6.3V_X5R 0603
CB4 1UF_10V_X5R 0603
C780 1UF_6.3V_X5R
C794 1UF_6.3V_X5R
PLACE NEAR DIMM AREA
M_RESET_N
C60 X_220PF_50V_NPO
NC
For Intel MOW

| | | | |
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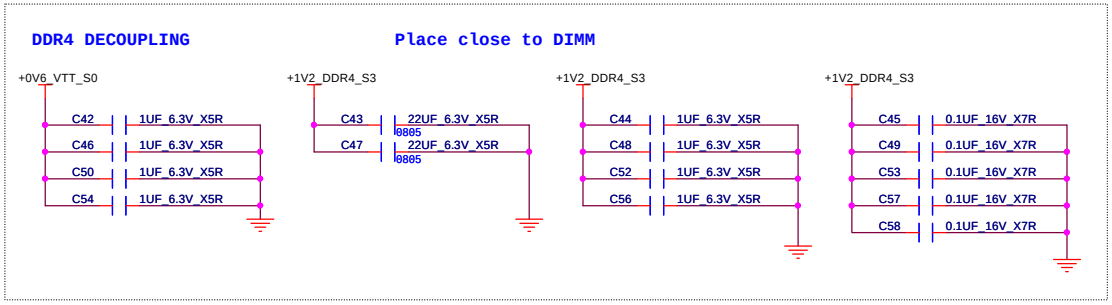
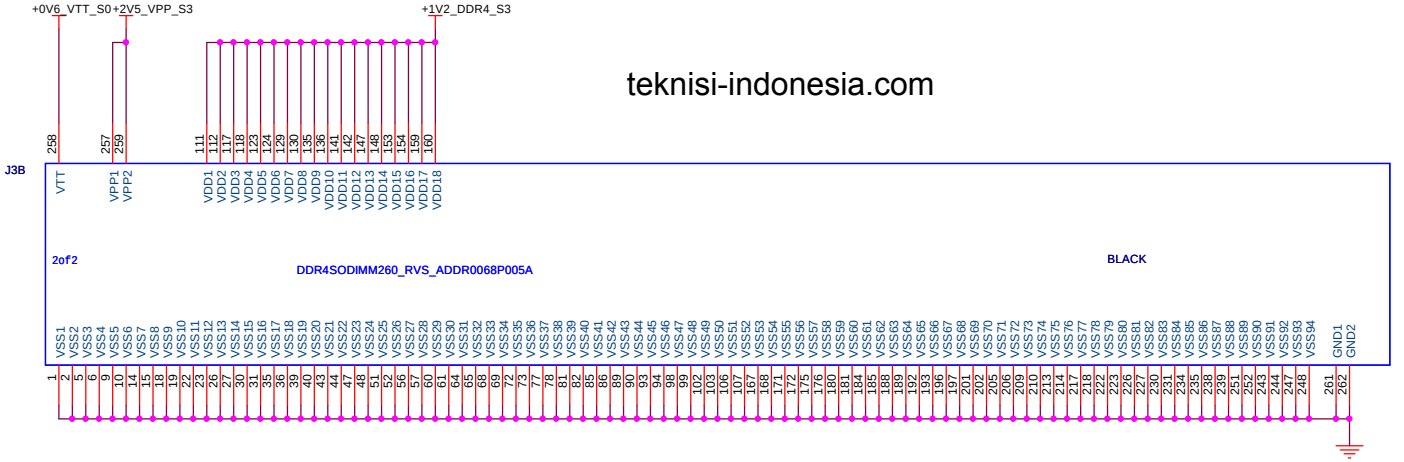
# DDR4 SO-DIMM CHANNEL A

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# DDR4 SO-DIMM CHANNEL B

## CHANNEL B
## ADDRESS:0XA4 010

## DIMM2

CAD Note:
all signal should have
10 mil trace width

M_B_DQS_DP8 M_B_DQS_DN8 M_B_DQS_DP7 M_B_DQS_DN7 M_B_DQS_DP6 M_B_DQS_DN6 M_B_DQS_DP5 M_B_DQS_DN5 M_B_DQS_DP4 M_B_DQS_DN4 M_B_DQS_DP3 M_B_DQS_DN3 M_B_DQS_DP2 M_B_DQS_DN2 M_B_DQS_DP1 M_B_DQS_DN1 M_B_DQS_DP0 M_B_DQS_DN0 M_B_ODT1 M_B_ODT0

+1V2_DDR4_S3

R69 240R_1% 0402

M_B_TS_EVENT_N

M_B_DATA_CB[7..0]

M_B_DATA_CB0 M_B_DATA_CB1 M_B_DATA_CB2 M_B_DATA_CB3 M_B_DATA_CB4 M_B_DATA_CB5 M_B_DATA_CB6 M_B_DATA_CB7

M_B_DQ[63..0]

J4A

1of2

DDR4SODIMM260_RVS_ADDR0072P005A BLACK

M_B_PARITY M_ALERT_B_N M_B_ACT_N M_B_BG0 M_B_BG1

M_B_CLK_DP0 M_B_CLK_DN0 M_B_CLK_DP1 M_B_CLK_DN1

M_RESET_N M_B_CS_N[1..0] M_B_CKE[1..0] M_B_BA[1..0] SMB_DATA SMB_CLK

M_B_MA[16..0]

+3V_S0

R70 0R

C86

CAD NOTE:
PLACE RESISTORS
CLOSE TO CH_A DIMMS
ON DIMM_VREF_A

DIMM_DQ_CPU_VREF_B

R66 2R_1% 0402

DIMM_CA_VREF_B

C41 0.022UF_16V_X7R

DIMM_CA_CPU_VREF_RC_B

R68 24R9_1% 0402

C2176 4.7UF_6.3V_X5R 0603

CB5 1UF_10V_X5R 0603

C786 1UF_6.3V_X5R

C800 1UF_6.3V_X5R

R60 1K_1%

R64 1K_1%

C2725 1UF_6.3V_X5R

PLACE NEAR DIMM AREA

M_RESET_N

C59 X_220PF_50V_NPO

NC
For Intel MOW

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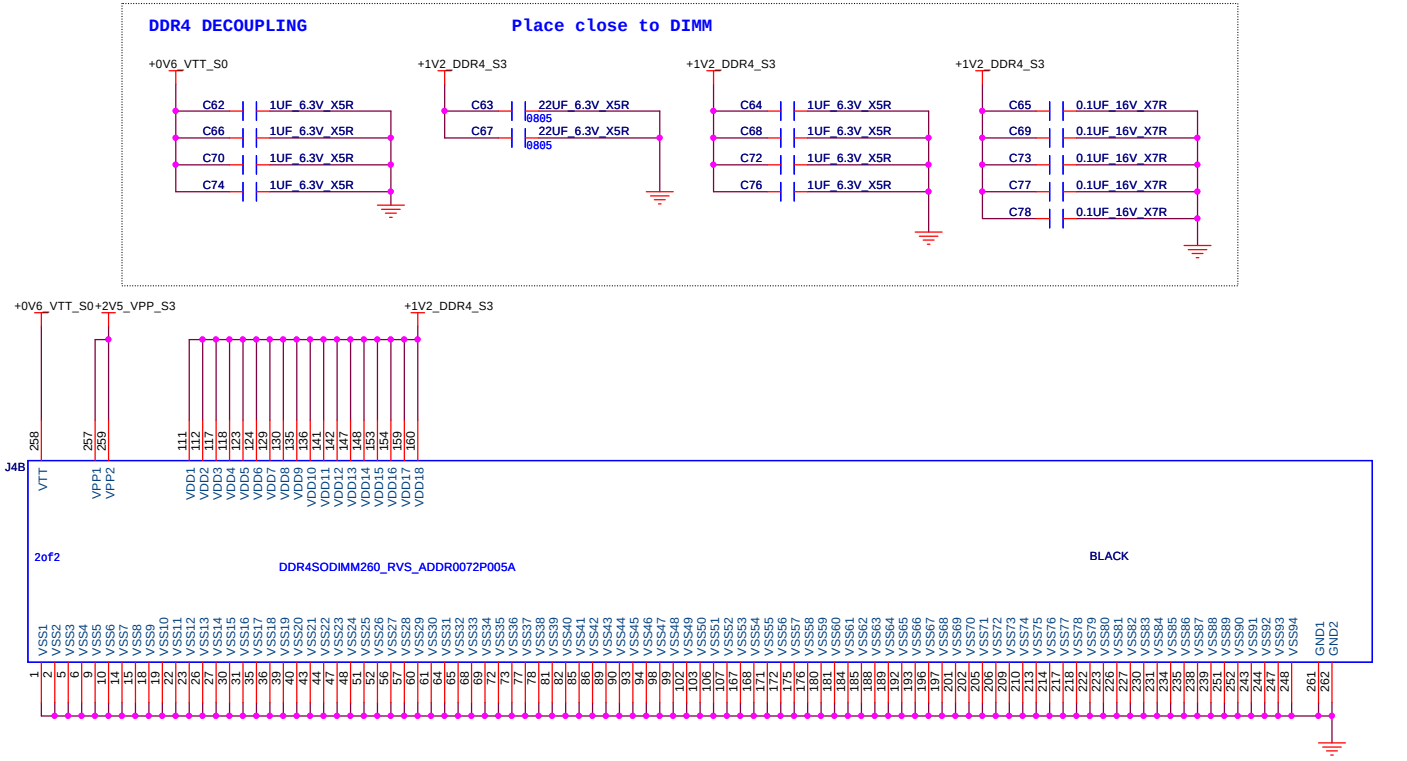
# DDR4 SO-DIMM CHANNEL B

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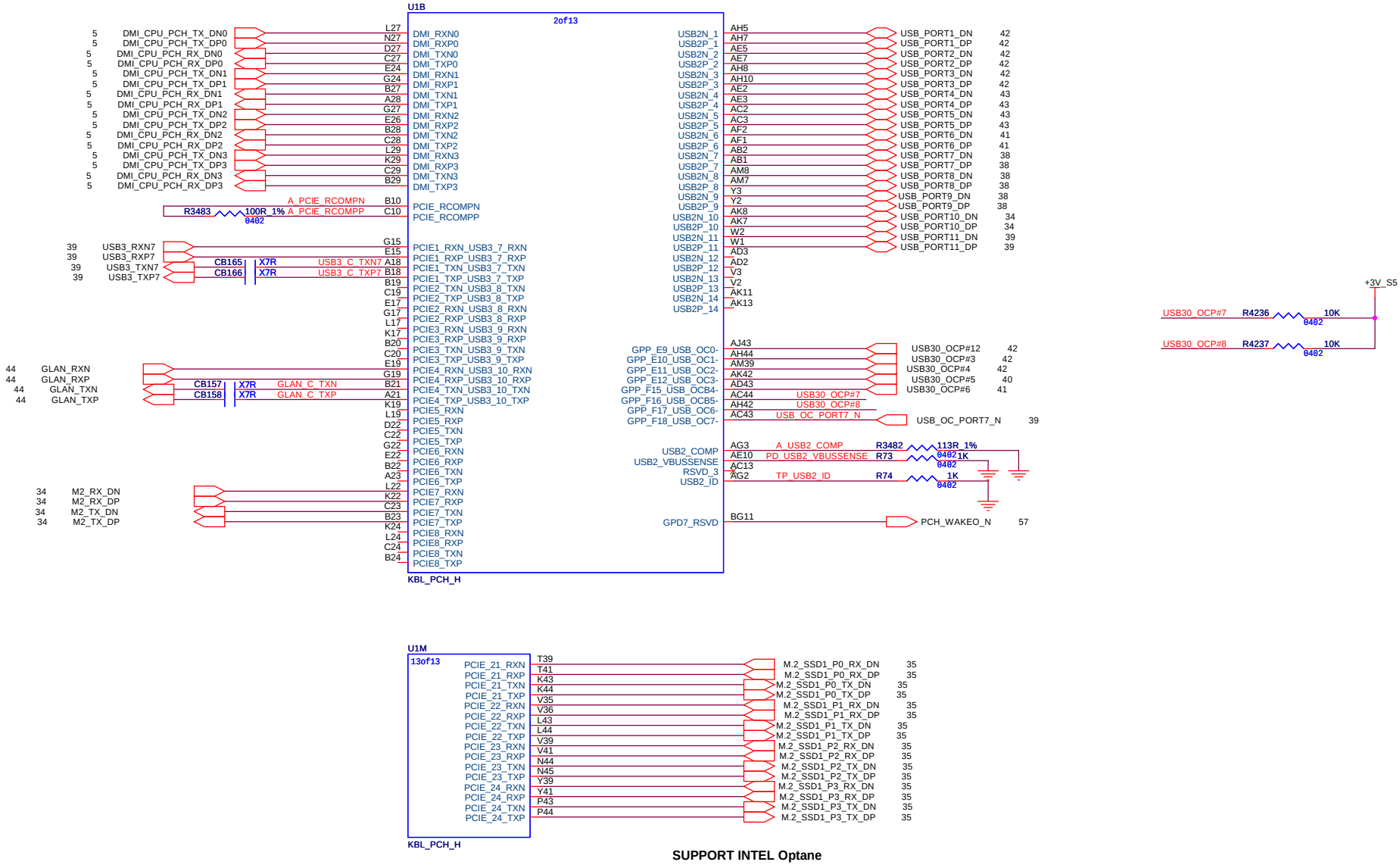


**SUPPORT INTEL Optane**

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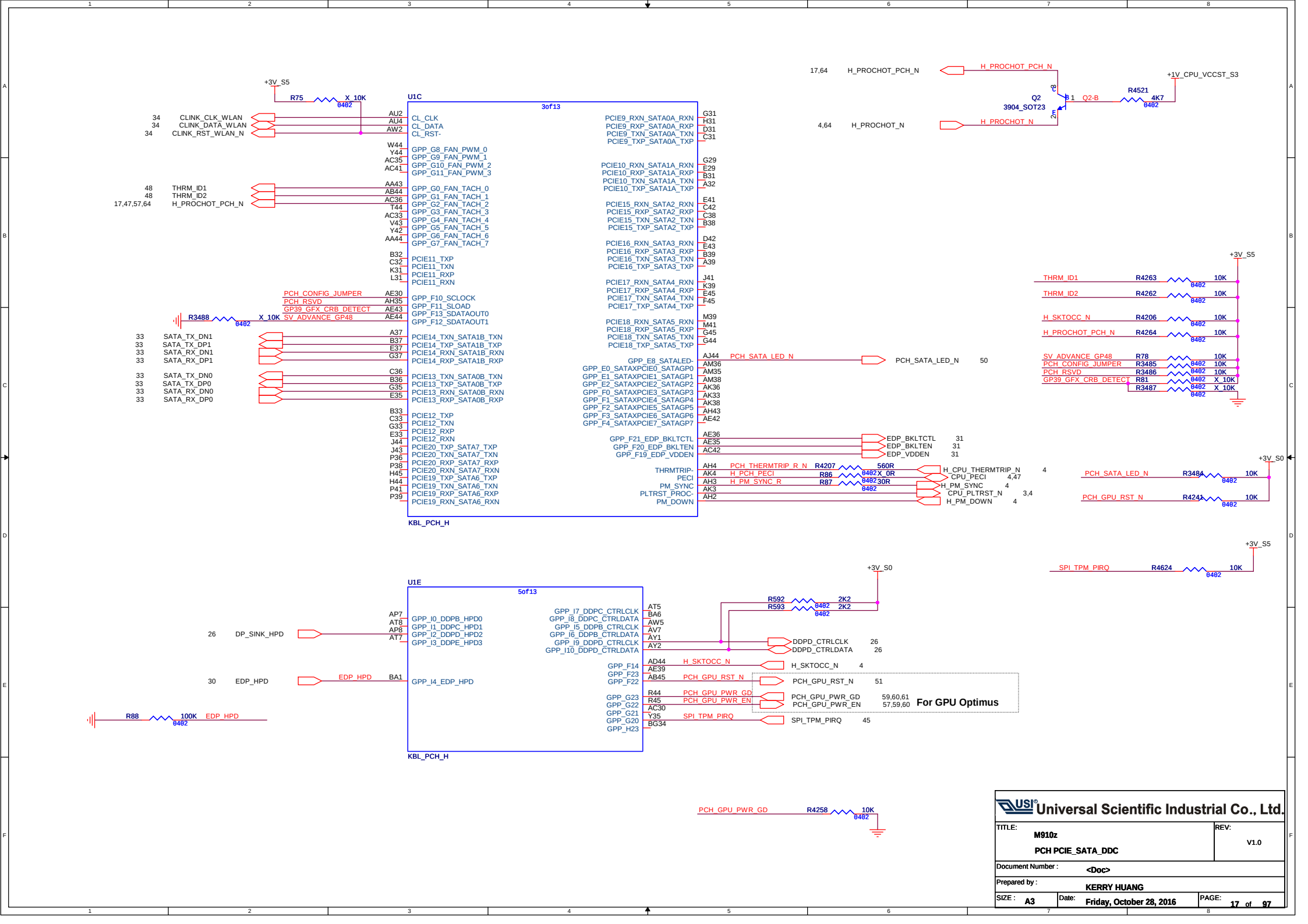


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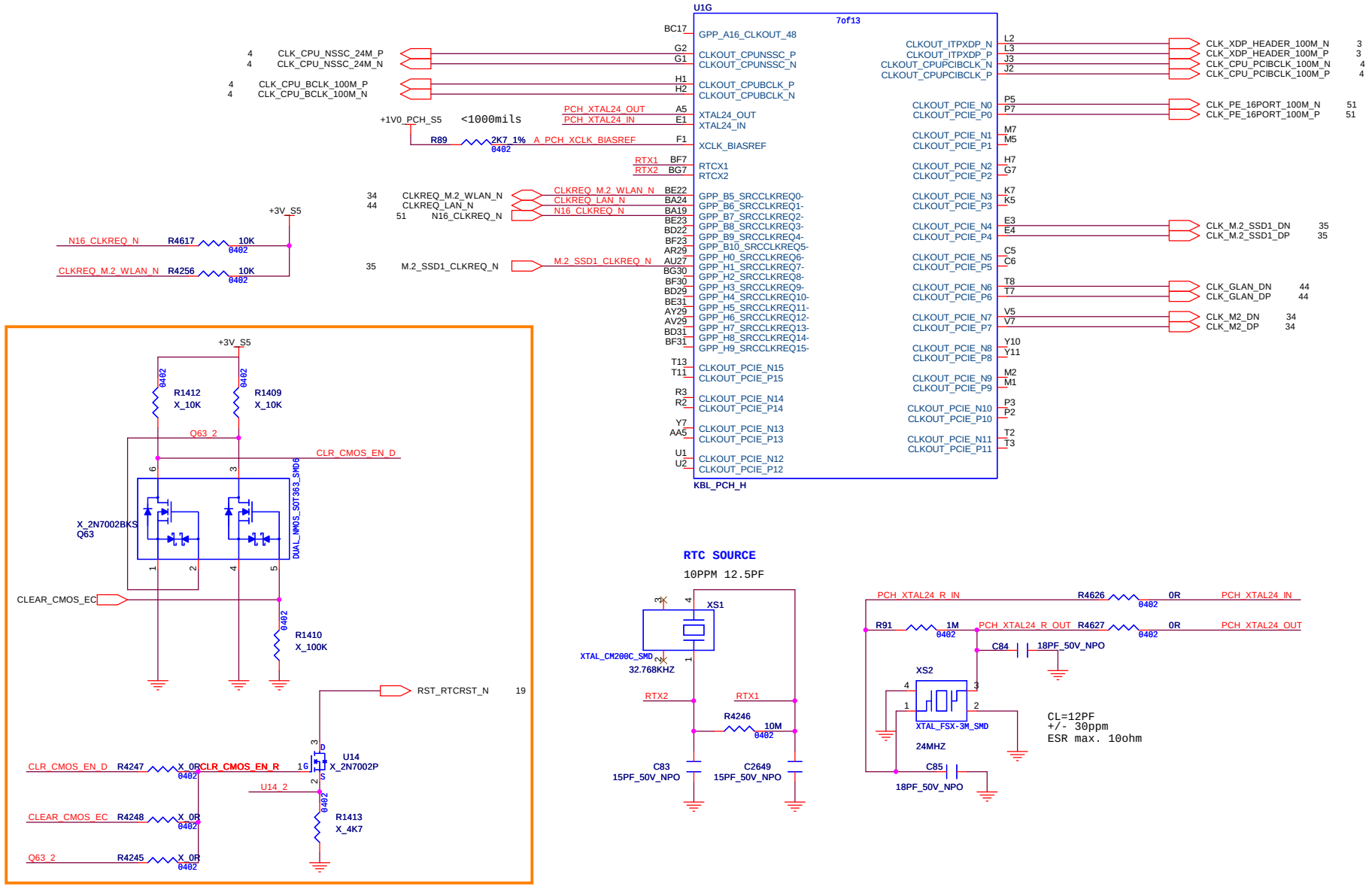
# PCH CLOCK

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| SIZE : A3 | Date: Friday, October 28, 2016 |
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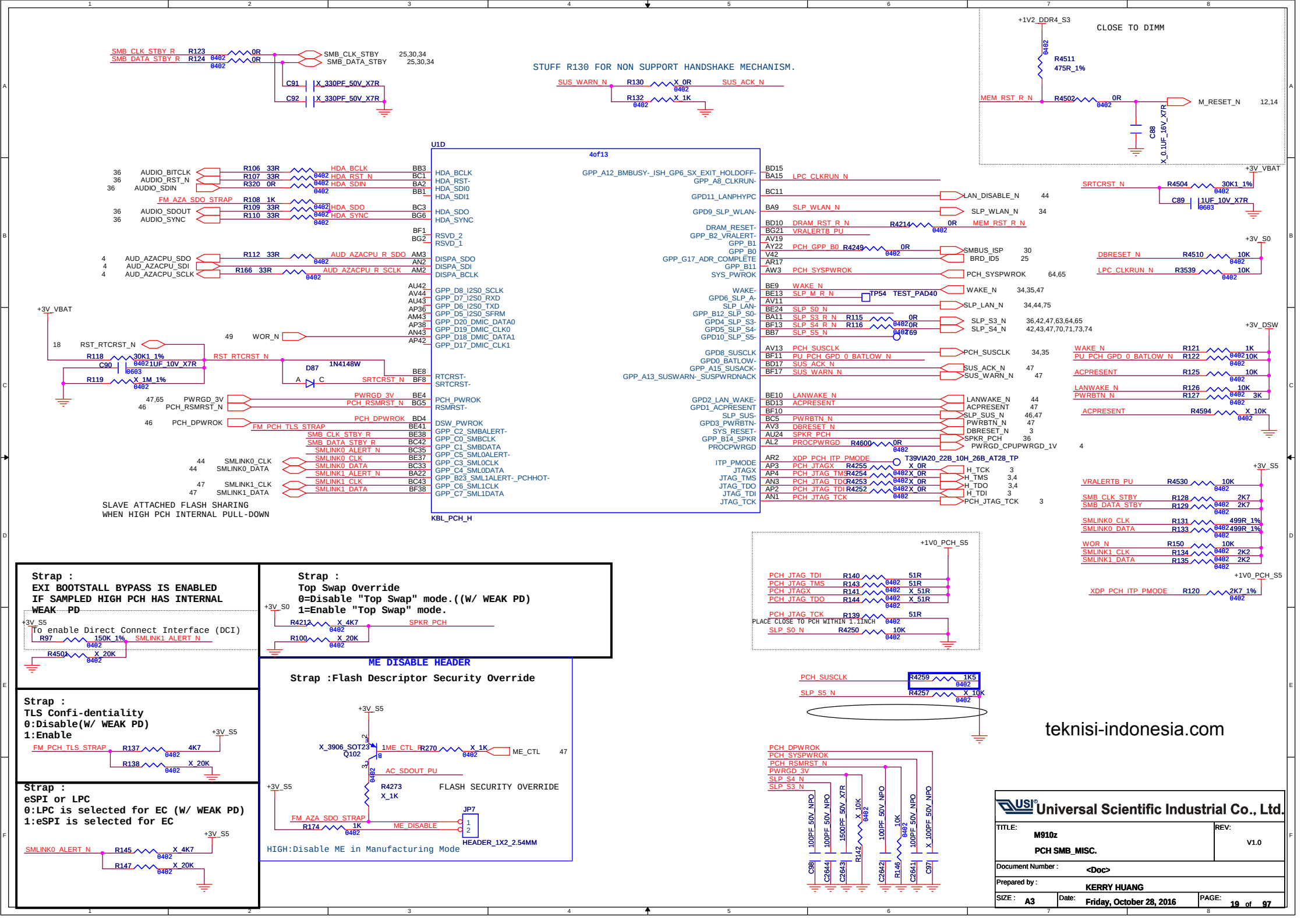
SMB_CLK_STBY_R R123 0R
SMB_DATA_STBY_R R124 0R
SMB_CLK_STBY 25,30,34
SMB_DATA_STBY 25,30,34
C91 X_330PF_50V_X7R
C92 X_330PF_50V_X7R
STUFF R130 FOR NON SUPPORT HANDSHAKE MECHANISM.
SUS_WARN_N R130 X_0R SUS_ACK_N
R132 X_1K
+1V2_DDR4_S3
CLOSE TO DIMM
R4511 475R_1%
MEM_RST_R_N R4502 0R M_RESET_N 12,14
C88 X_0.1UF_16V_X7R
U1D
4of13
KBL_PCH_H
HDA_BCLK
HDA_RST-
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
RSVD_2
RSVD_1
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8_I2S0_SCLK
GPP_D7_I2S0_RXD
GPP_D6_I2S0_TXD
GPP_D5_I2S0_SFRM
GPP_D20_DMIC_DATA0
GPP_D19_DMIC_CLK0
GPP_D18_DMIC_DATA1
GPP_D17_DMIC_CLK1
RTCRST-
SRTCRST-
PCH_PWROK
RSMRST-
DSW_PWROK
GPP_C2_SMBALERT-
GPP_C0_SMBCLK
GPP_C1_SMBDATA
GPP_C5_SML0ALERT-
GPP_C3_SML0CLK
GPP_C4_SML0DATA
GPP_B23_SML1ALERT-_PCHHOT-
GPP_C6_SML1CLK
GPP_C7_SML1DATA
GPP_A12_BMBUSY-_ISH_GP6_SX_EXIT_HOLDOFF-
GPP_A8_CLKRUN-
GPD11_LANPHYPC
GPD9_SLP_WLAN-
DRAM_RESET-
GPP_B2_VRALERT-
GPP_B1
GPP_B0
GPP_G17_ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE-
GPD6_SLP_A-
SLP_LAN-
GPP_B12_SLP_S0-
GPD4_SLP_S3-
GPD5_SLP_S4-
GPD10_SLP_S5-
GPD8_SUSCLK
GPD0_BATLOW-
GPP_A15_SUSACK-
GPP_A13_SUSWARN-_SUSPWRDNACK
GPD2_LAN_WAKE-
GPD1_ACPRESENT
SLP_SUS-
GPD3_PWRBTN-
SYS_RESET-
GPP_B14_SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
LPC_CLKRUN_N
LAN_DISABLE_N 44
SLP_WLAN_N
SLP_WLAN_N 34
DRAM_RST_R_N R4214 0R MEM_RST_R_N
VRALERTB_PU
PCH_GPP_B0 R4249 0R
SMBUS_ISP 30
BRD_ID5 25
PCH_SYSPWROK
PCH_SYSPWROK 64,65
WAKE_N
SLP_M_R_N TP54 TEST_PAD40
WAKE_N 34,35,47
SLP_LAN_N 34,44,75
SLP_S0_N
SLP_S3_N R115 0R
SLP_S4_N R116 0R
SLP_S3_N 36,42,47,63,64,65
SLP_S4_N 42,43,47,70,71,73,74
SLP_S5_N R4769
PCH_SUSCLK
PU_PCH_GPD_0_BATLOW_N
SUS_ACK_N
SUS_WARN_N
SUS_ACK_N 47
SUS_WARN_N 47
LANWAKE_N
ACPRESENT
SLP_SUS_N
PWRBTN_N
DBRESET_N
SPKR_PCH
PROCPWRGD R4600 0R
LANWAKE_N 44
ACPRESENT 47
SLP_SUS_N 46,47
PWRBTN_N 47
DBRESET_N 3
SPKR_PCH 36
PWRGD_CPUPWRGD_1V 4
XDP_PCH_ITP_PMODE T39VIA20_22B_10H_26B_AT28_TP
PCH_JTAGX R4255 X_0R
PCH_JTAG_TMS R4254 X_0R
PCH_JTAG_TDO R4253 X_0R
PCH_JTAG_TDI R4252 X_0R
PCH_JTAG_TCK
H_TCK 3
H_TMS 3,4
H_TDO 3,4
H_TDI 3
PCH_JTAG_TCK 3
+3V_VBAT
SRTCRST_N R4504 30K1_1%
C89 1UF_10V_X7R
+3V_S0
DBRESET_N R4510 10K
LPC_CLKRUN_N R3539 10K
+3V_DSW
WAKE_N R121 1K
PU_PCH_GPD_0_BATLOW_N R122 10K
ACPRESENT R125 10K
LANWAKE_N R126 10K
PWRBTN_N R127 3K
ACPRESENT R4594 X_10K
+3V_S5
VRALERTB_PU R4530 10K
SMB_CLK_STBY R128 2K7
SMB_DATA_STBY R129 2K7
SMLINK0_CLK R131 499R_1%
SMLINK0_DATA R133 499R_1%
WOR_N R150 10K
SMLINK1_CLK R134 2K2
SMLINK1_DATA R135 2K2
+1V0_PCH_S5
XDP_PCH_ITP_PMODE R120 2K7_1%
AUDIO_BITCLK R106 33R HDA_BCLK BB3
AUDIO_RST_N R107 33R HDA_RST_N BC1
AUDIO_SDIN R320 0R HDA_SDIN BA2
FM_AZA_SDO_STRAP R108 1K BB1
AUDIO_SDOUT R109 33R HDA_SDO BC3
AUDIO_SYNC R110 33R HDA_SYNC BG6
BF1
BG2
AUD_AZACPU_SDO R112 33R AUD_AZACPU_R_SDO AM3
AUD_AZACPU_SDI AN2
AUD_AZACPU_SCLK R166 33R AUD_AZACPU_R_SCLK AM2
AU42
AV44
AU43
AP36
AM43
AP38
AN43
AP42
WOR_N
+3V_VBAT
RST_RTCRST_N
R118 30K1_1%
C90 1UF_10V_X7R
R119 X_1M_1%
RST_RTCRST_N
D87 1N4148W
SRTCRST_N
BE8
BF8
PWRGD_3V
PCH_RSMRST_N
BE4
BG5
PCH_DPWROK
BD4
FM_PCH_TLS_STRAP
BE41
SMB_CLK_STBY_R
BE38
SMB_DATA_STBY_R
BC42
SMLINK0_ALERT_N
BC35
SMLINK0_CLK
BE37
SMLINK0_DATA
BC33
SMLINK1_ALERT_N
BA22
SMLINK1_CLK
BC43
SMLINK1_DATA
BF38
SLAVE ATTACHED FLASH SHARING
WHEN HIGH PCH INTERNAL PULL-DOWN
Strap :
EXI BOOTSTALL BYPASS IS ENABLED
IF SAMPLED HIGH PCH HAS INTERNAL
WEAK PD
To enable Direct Connect Interface (DCI)
R97 150K_1%
R4501 X_20K
Strap :
Top Swap Override
0=Disable "Top Swap" mode.((W/ WEAK PD)
1=Enable "Top Swap" mode.
R4212 X_4K7
R100 X_20K
SPKR_PCH
ME DISABLE HEADER
Strap :Flash Descriptor Security Override
X_3906_SOT23 Q102
1ME_CTL_R270 X_1K
ME_CTL 47
AC_SDOUT_PU
R4273 X_1K
FLASH SECURITY OVERRIDE
FM_AZA_SDO_STRAP
R174 1K
ME_DISABLE
JP7
HEADER_1X2_2.54MM
HIGH:Disable ME in Manufacturing Mode
Strap :
TLS Confi-dentiality
0:Disable(W/ WEAK PD)
1:Enable
FM_PCH_TLS_STRAP R137 4K7
R138 X_20K
Strap :
eSPI or LPC
0:LPC is selected for EC (W/ WEAK PD)
1:eSPI is selected for EC
SMLINK0_ALERT_N R145 X_4K7
R147 X_20K
PCH_JTAG_TDI R140 51R
PCH_JTAG_TMS R143 51R
PCH_JTAGX R141 X_51R
PCH_JTAG_TDO R144 X_51R
PCH_JTAG_TCK R139 51R
PLACE CLOSE TO PCH WITHIN 1.1INCH
SLP_S0_N R4250 10K
PCH_SUSCLK R4259 1K5
SLP_S5_N R4257 X_10K
PCH_DPWROK
PCH_SYSPWROK
PCH_RSMRST_N
PWRGD_3V
SLP_S4_N
SLP_S3_N
100PF_50V_NPO C98
100PF_50V_NPO C2644
1500PF_50V_X7R C2643
X_10K R142
100PF_50V_NPO C2642
10K R146
100PF_50V_NPO C2641
X_100PF_50V_NPO C97
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Universal Scientific Industrial Co., Ltd.
TITLE: M910z
PCH SMB_MISC.
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
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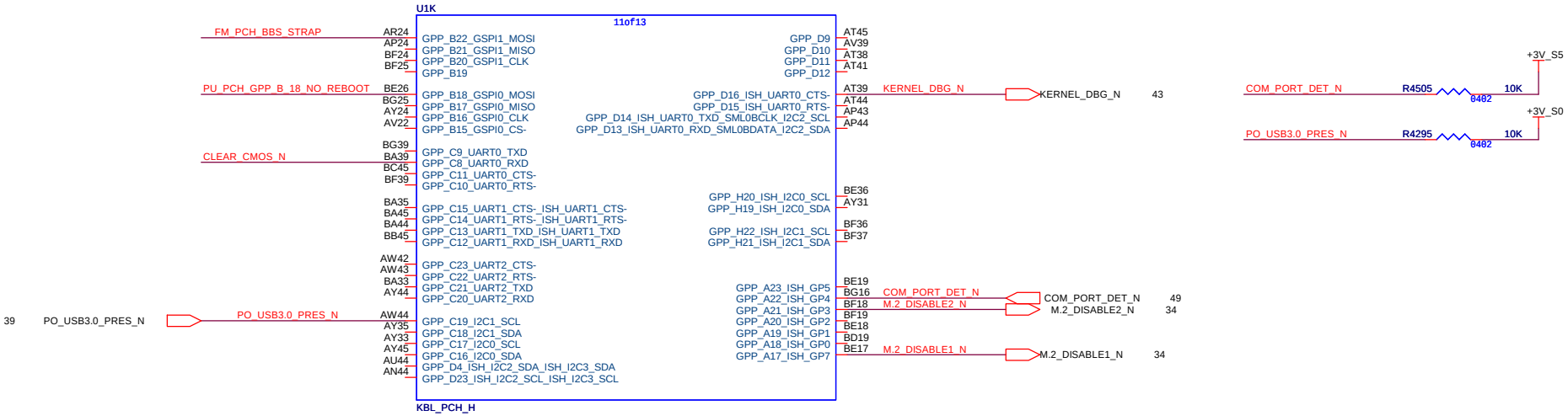
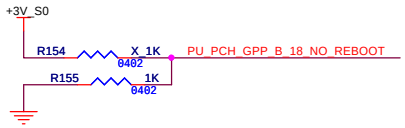
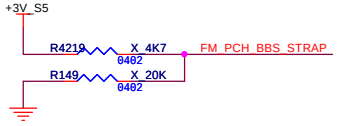


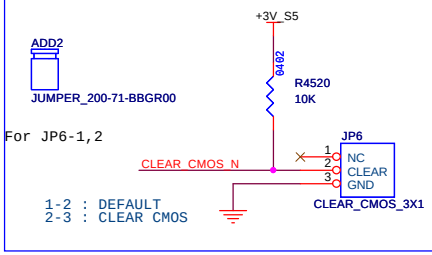

**Strap :**
**No Reboot**
**0=Disable "No Reboot" mode(W/ WEAK PD)**
**1=Enable "No Reboot" mode**




**Strap :**
**Boot BIOS Strap Bit 10 BBS**
**0:SPI (W/ WEAK PD)**
**1:LPC**




**CLEAR CMOS**

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| TITLE: M910z<br>PCH HDA_SMB | REV: V1.0 |
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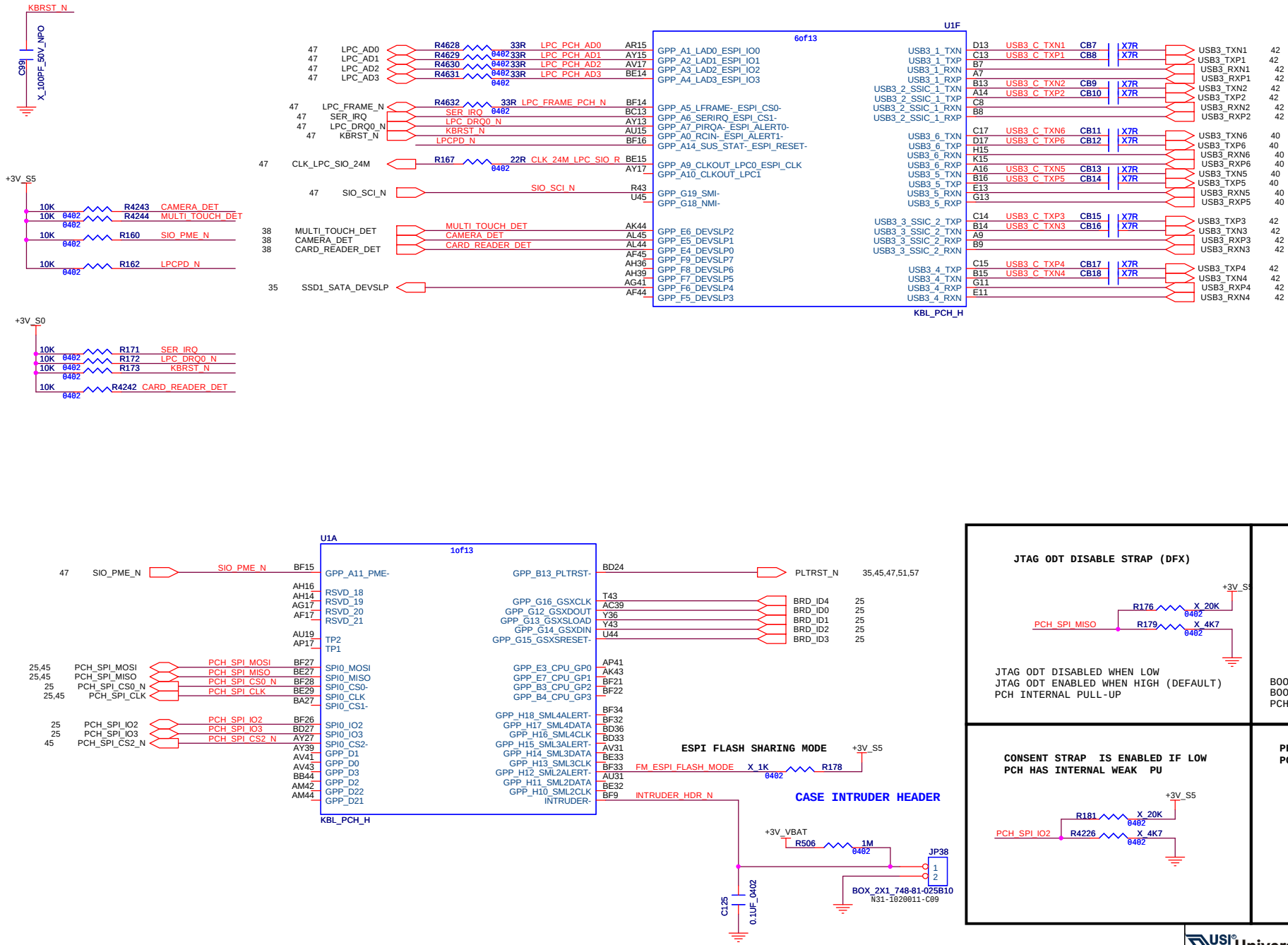


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| TITLE: M910z<br>PCH LPC_SPI_U3 | REV: V1.0 |
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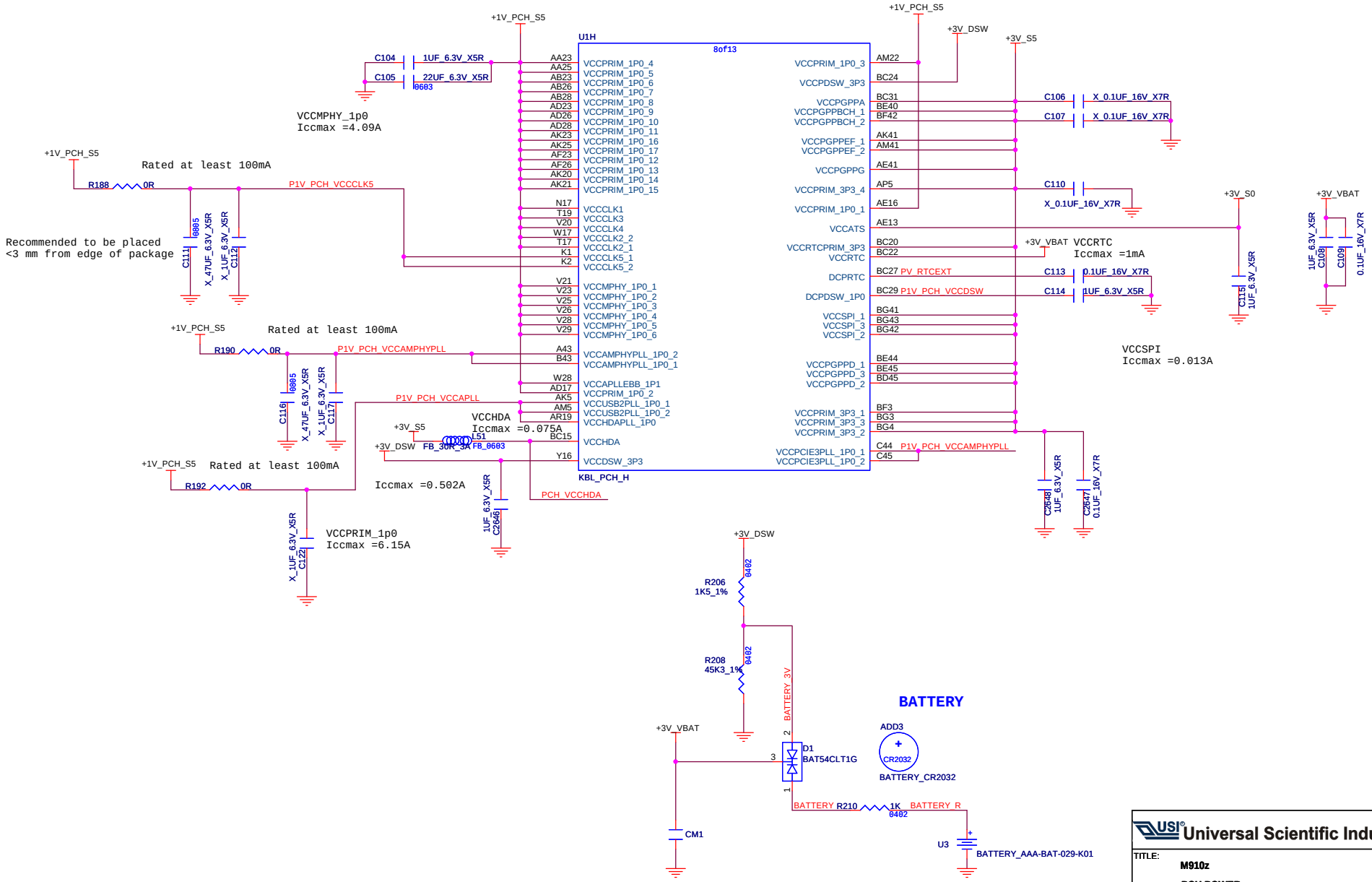


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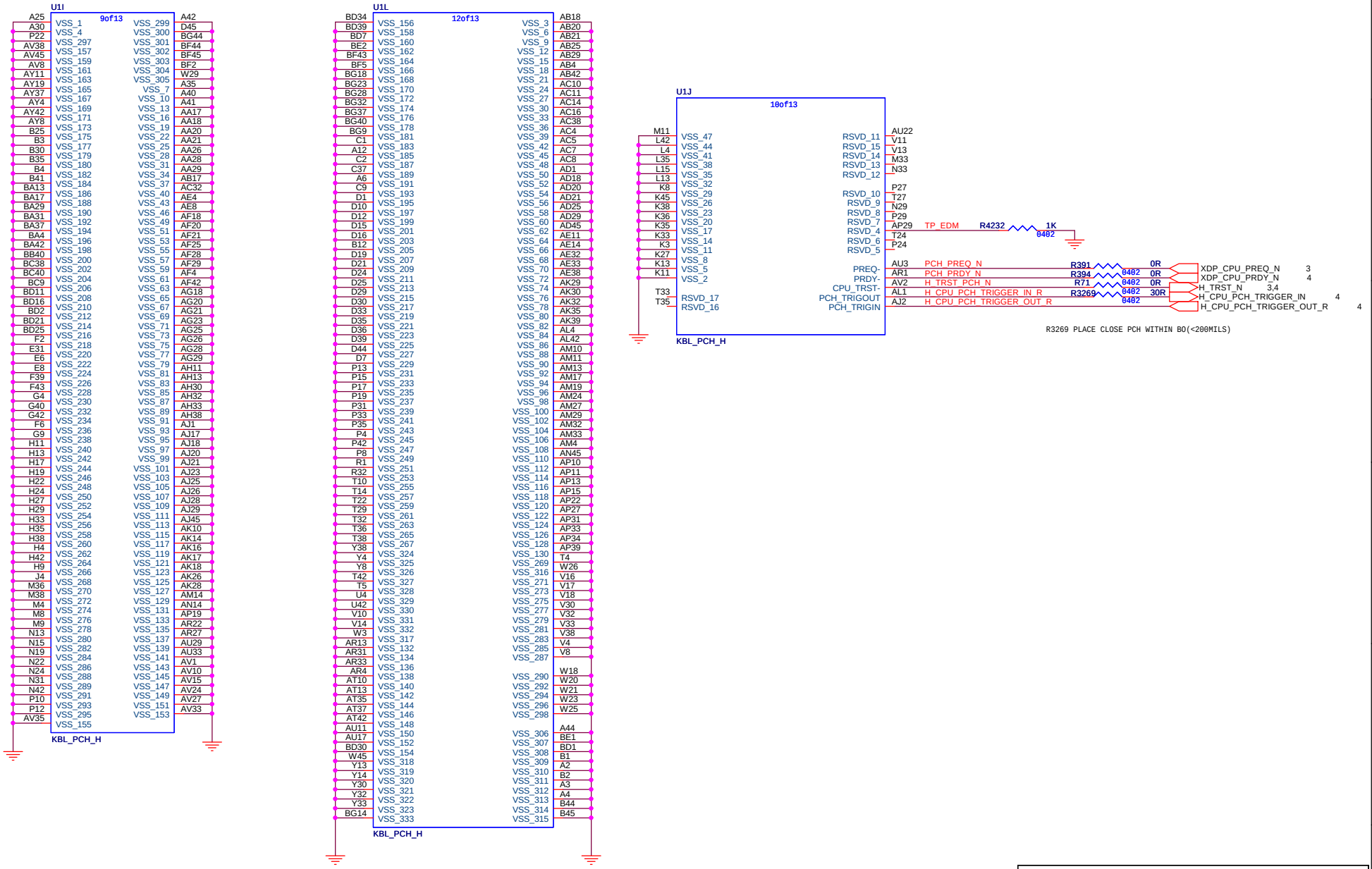


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| TITLE: M910z PCH GND | REV: V1.0 |
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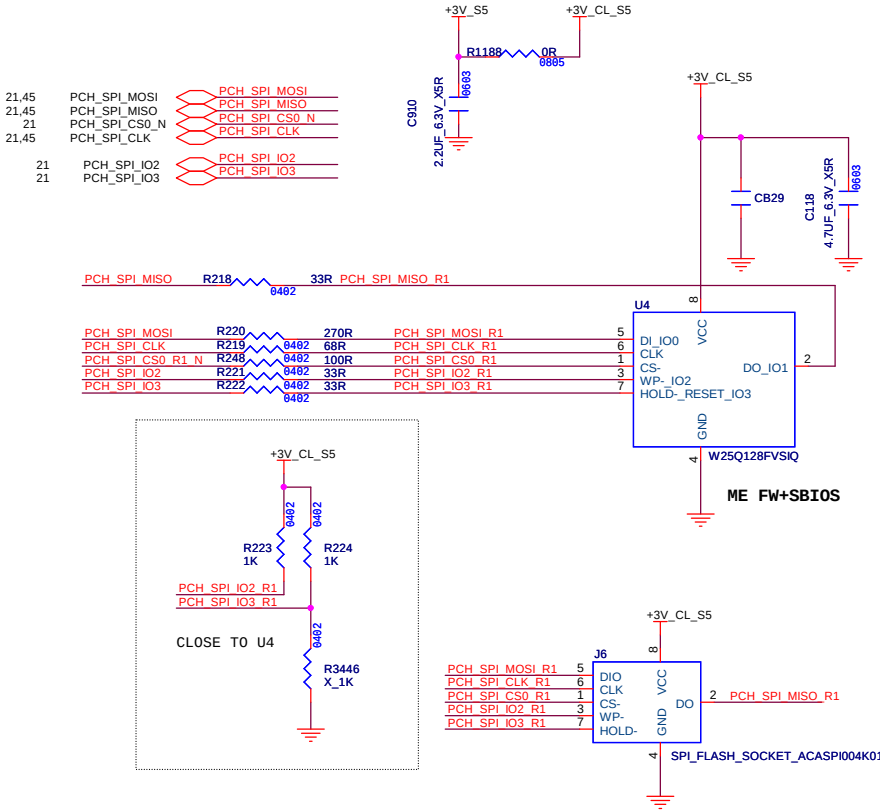
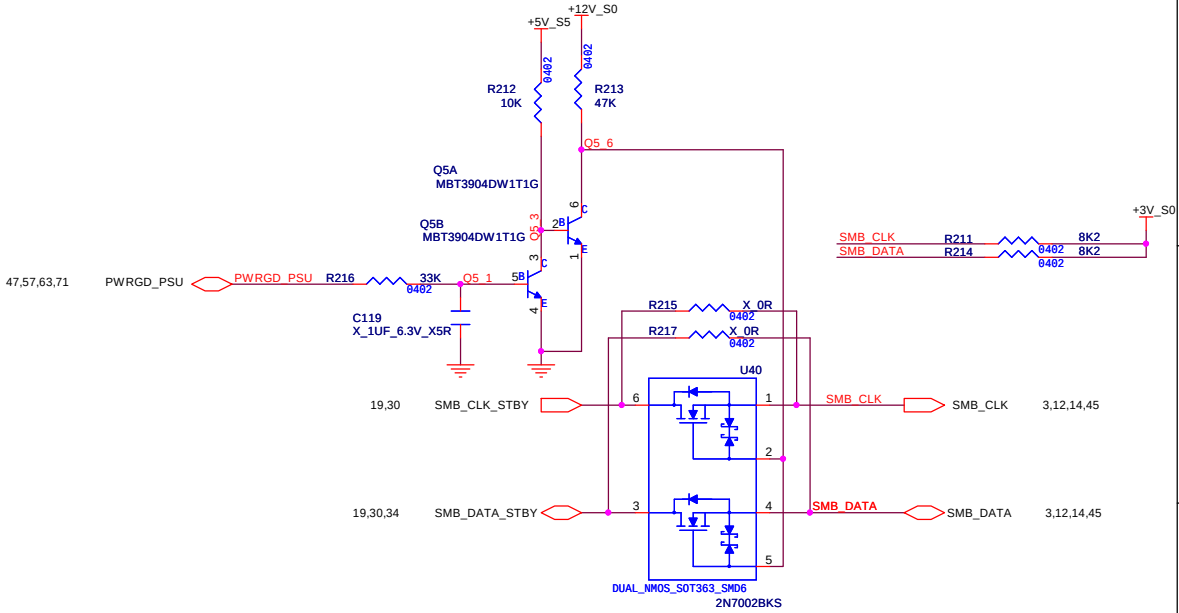
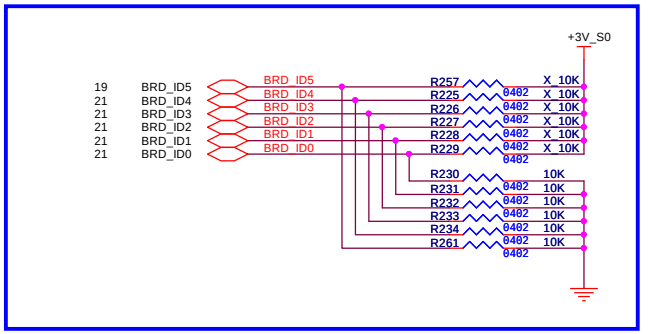
# SPI FLASH




# BOARD ID




| BOARD ID MAP | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | |
|---|---|---|---|---|---|---|---|
| M910Z W/GPU SURGE LC | 0 | 0 | 0 | 0 | 0 | 0 | default |
| M910Z W/O GPU NON-SURGE LI | 0 | 0 | 0 | 0 | 0 | 1 | |
| M810Z W/GPU LC | 0 | 0 | 0 | 0 | 1 | 0 | |
| M810Z WO/GPU LC | 0 | 0 | 1 | 0 | 1 | 1 | |
| M810Z WO/GPU LI | 0 | 0 | 1 | 1 | 0 | 0 | |
| M710Z W/O GPU LC | 0 | 0 | 1 | 1 | 0 | 1 | |
| M710Z W/O GPU LI | 0 | 0 | 1 | 1 | 1 | 0 | |

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|---|---|---|
| TITLE: M910z SPI & SMBUS & BOARD ID | | REV: V1.0 |
| Document Number : <Doc> | | |
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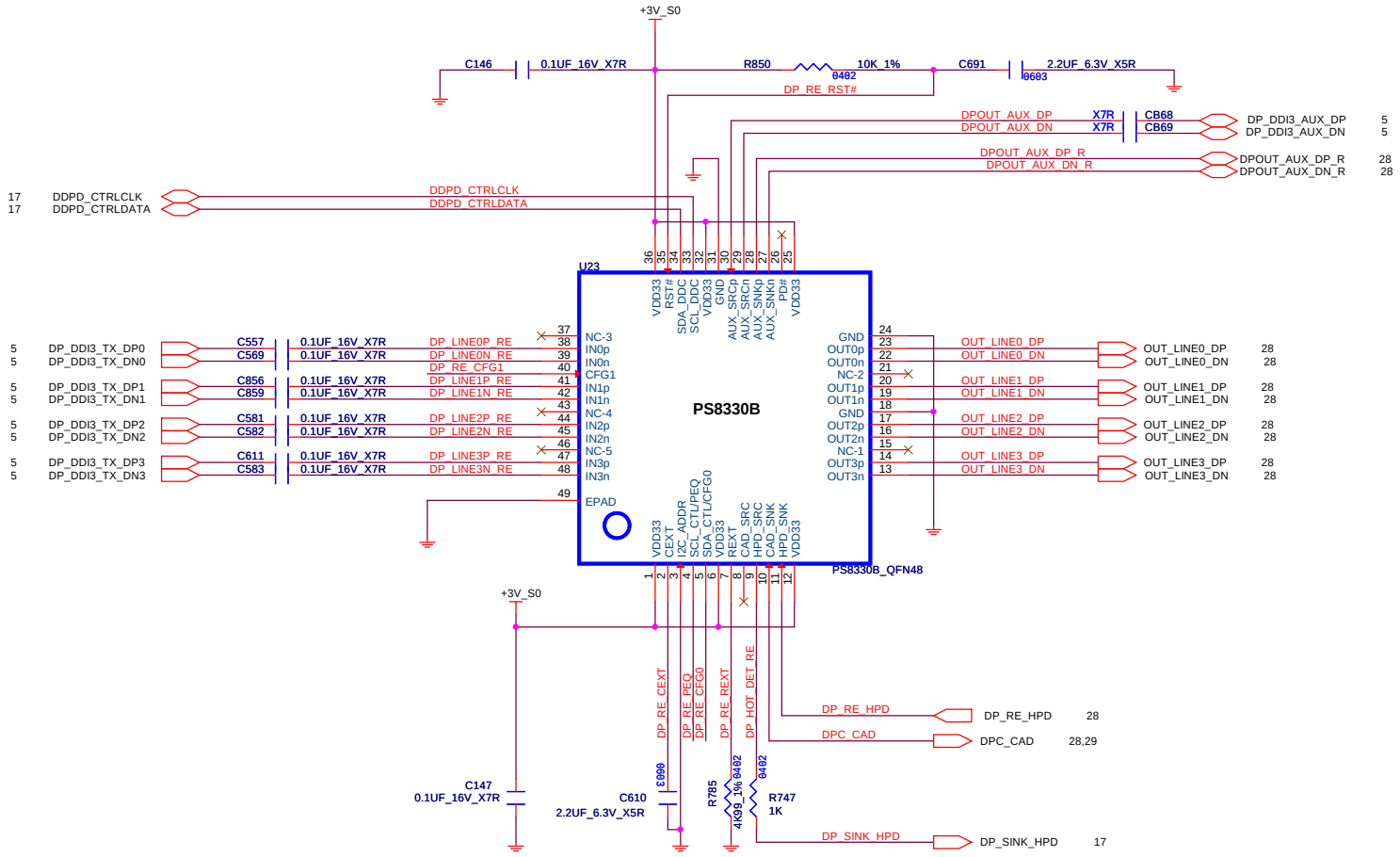
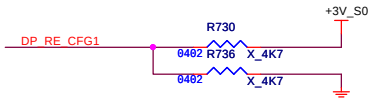
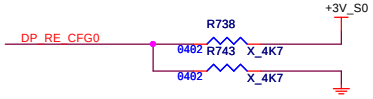
# DisplayPort Repeater

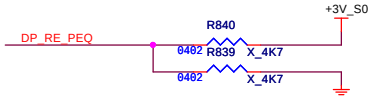



Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
In Pin Control Mode,
H: default, auto CTS test disable & input offset cancellation enable
L: auto CTS test enable & input offset cancellation enable
M: auto CTS test disable & input offset cancellation disable




CFG0: Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
CFG0 =
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing




PEQ: programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
PEQ =
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

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| TITLE: M910z DisplayPort Repeater | | | REV: V1.0 |
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| TITLE: M910z BLANK | | REV: V1.0 |
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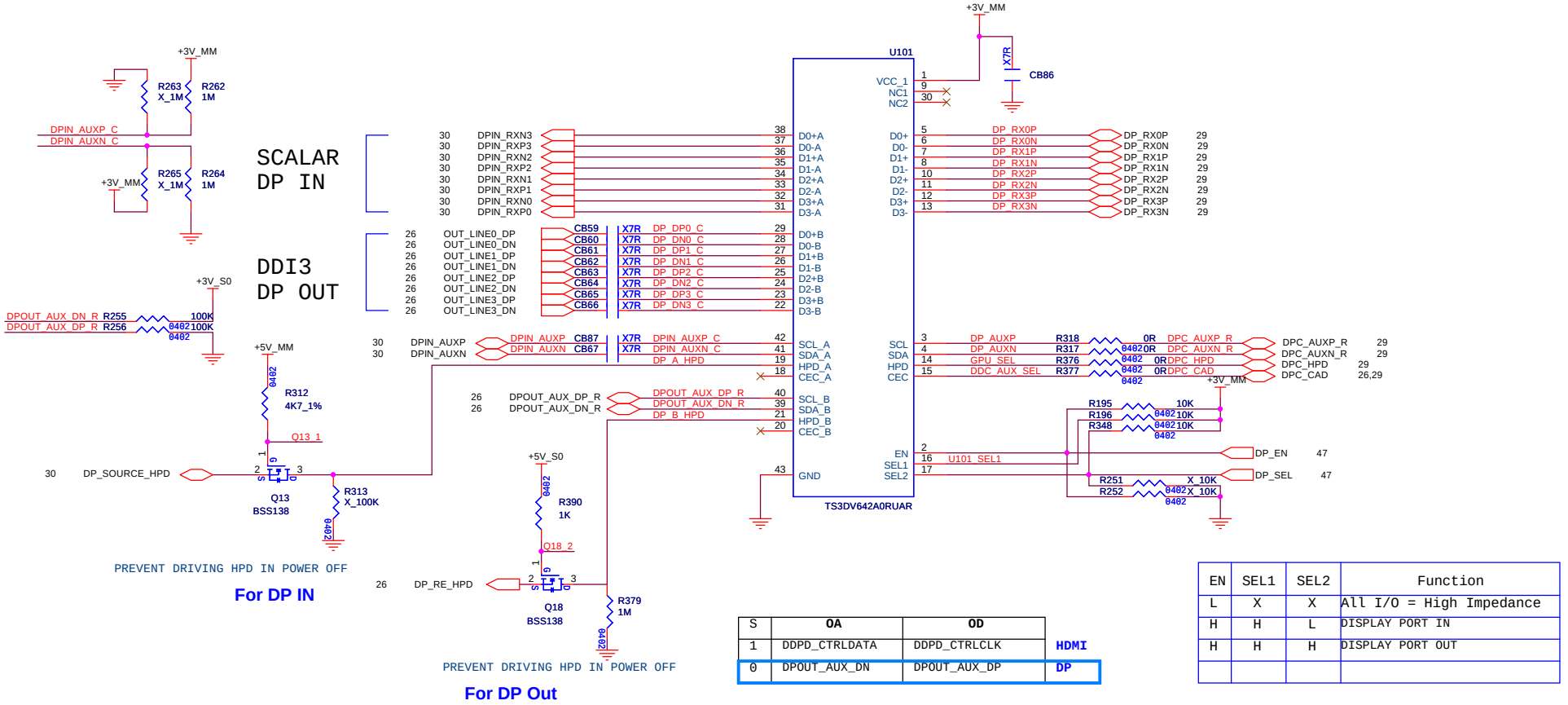


| S | OA | OD | |
|---|---|---|---|
| 1 | DDPD_CTRLDATA | DDPD_CTRLCLK | HDMI |
| 0 | DPOUT_AUX_DN | DPOUT_AUX_DP | DP |

| EN | SEL1 | SEL2 | Function |
|---|---|---|---|
| L | X | X | All I/O = High Impedance |
| H | H | L | DISPLAY PORT IN |
| H | H | H | DISPLAY PORT OUT |
| | | | |

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| TITLE: M910z<br>DP MUX/CONN | REV: V1.0 |
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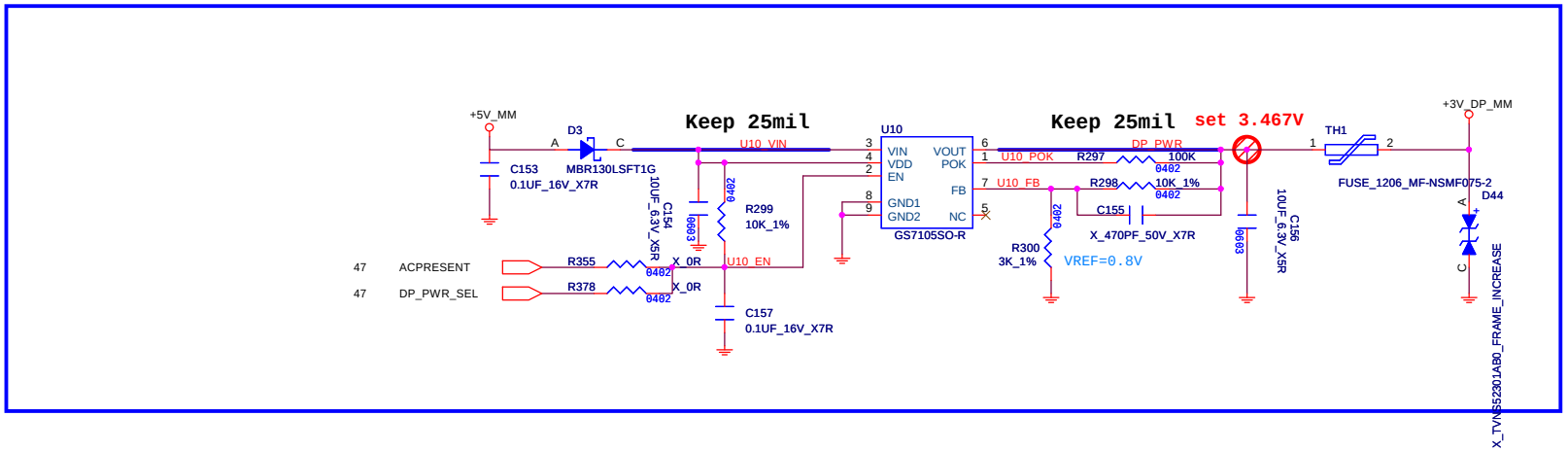
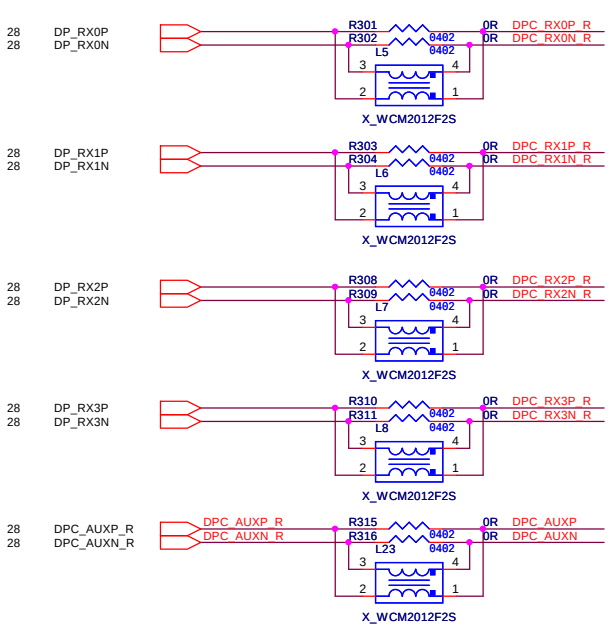
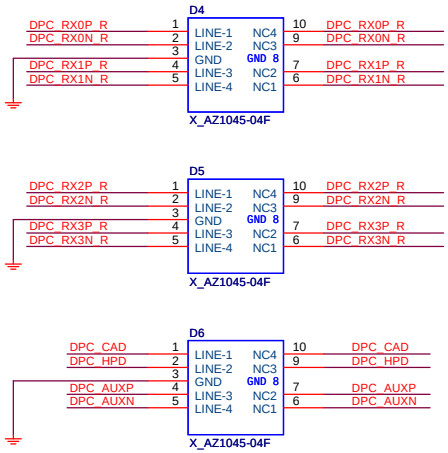
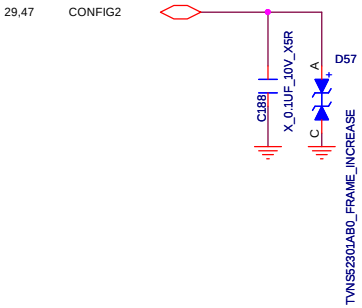


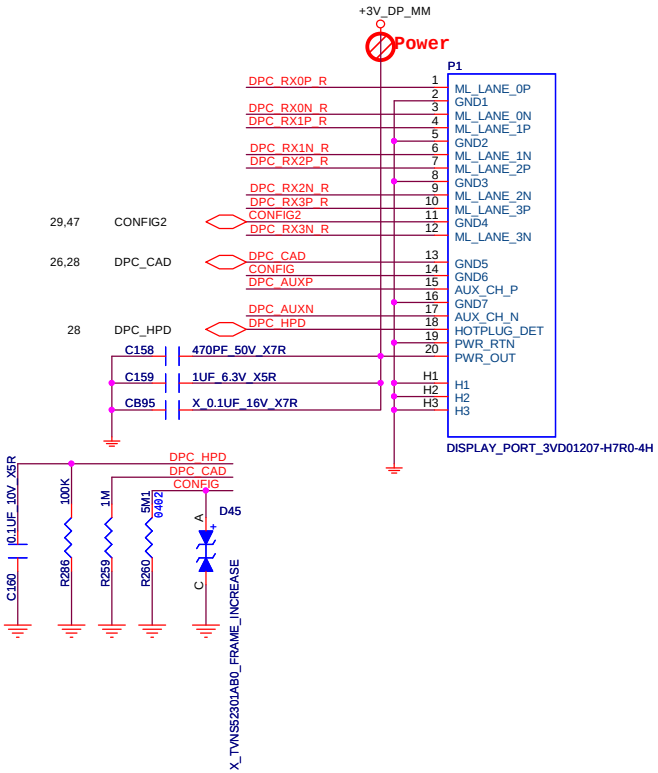

| Parameter | Value |
|---|---|
| Output voltage | 3.3V |
| Maximum output current | 0.5A |
| IC current limit | 3.5A |
| Max. PD(theoretically) | 0.85W |
| Rja | 75 °C/W |
| Enable condition | "+5V_MM" ON |

# DISPLAY PORT

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| TITLE: M910z DP PORT | | | REV: V1.0 |
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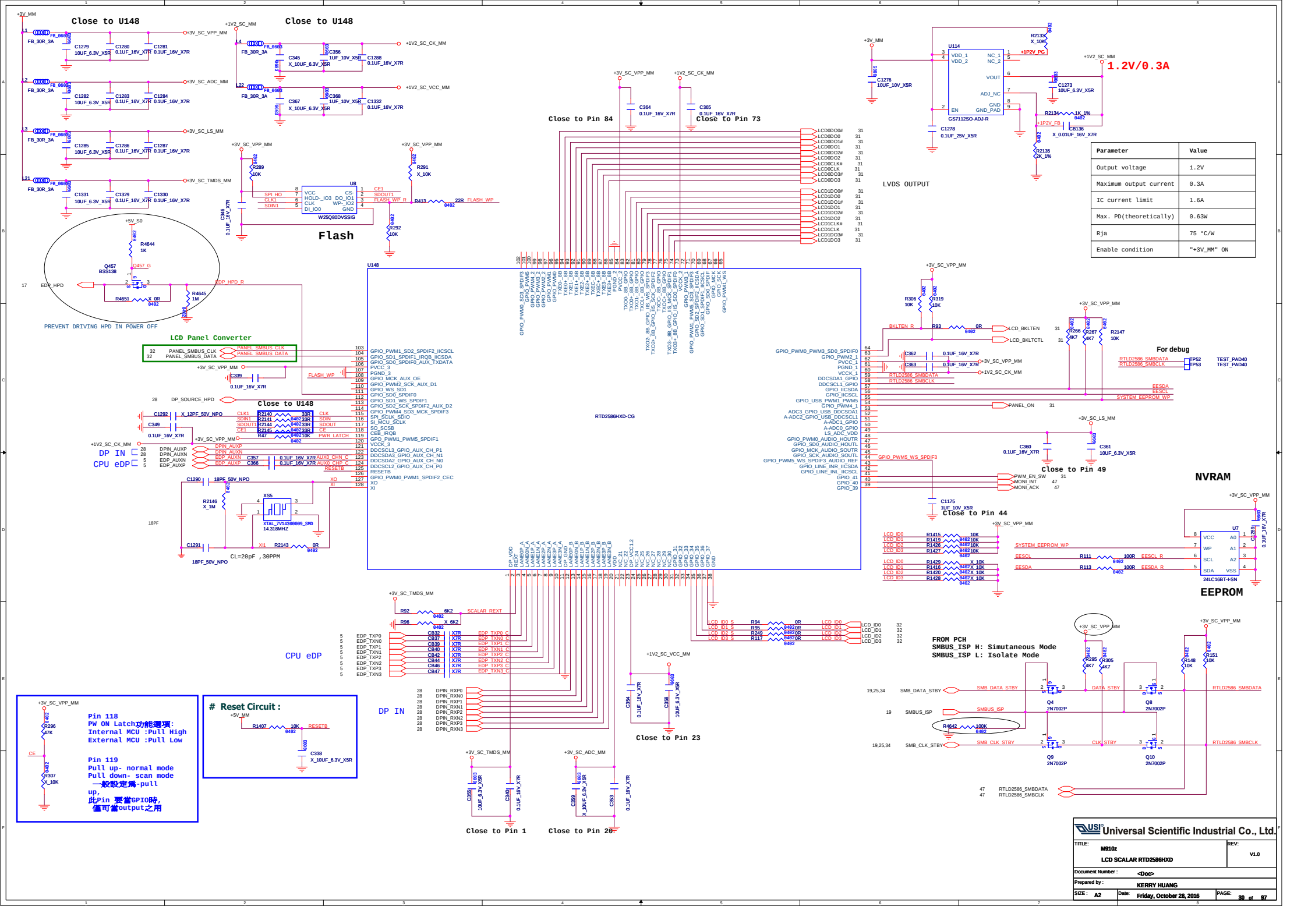
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 29 of 97 |




| Parameter | Value |
|---|---|
| Output voltage | 1.2V |
| Maximum output current | 0.3A |
| IC current limit | 1.6A |
| Max. PD(theoretically) | 0.63W |
| Rja | 75 °C/W |
| Enable condition | "+3V_MM" ON |

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|---|---|
| TITLE: M910z LCD SCALAR RTD2586HXD | REV: V1.0 |
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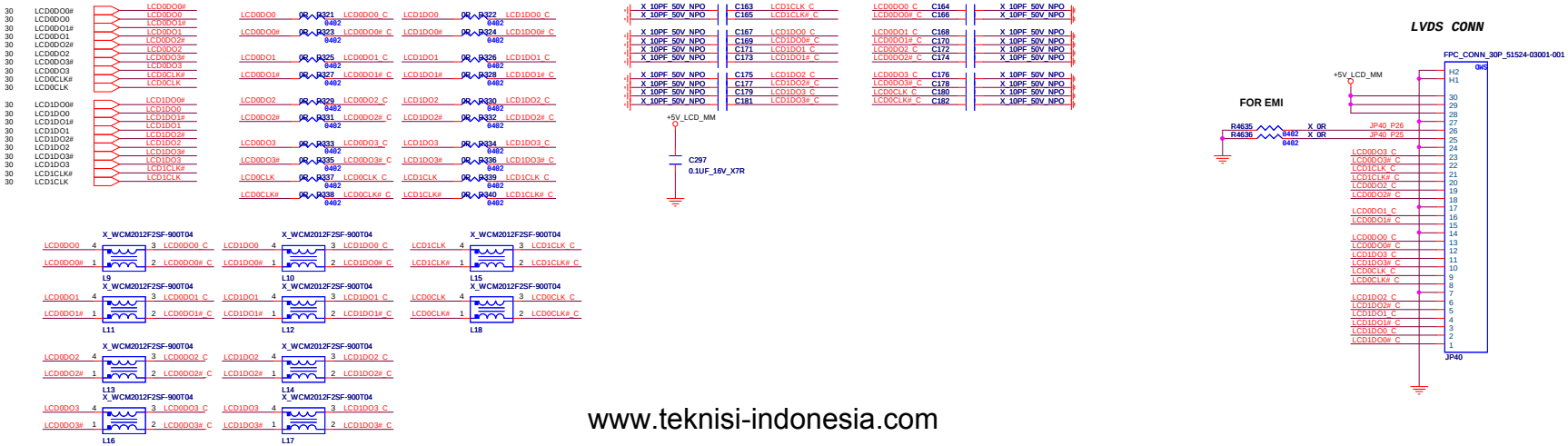
| Prepared by : KERRY HUANG | |
| SIZE : A2 | Date: Friday, October 28, 2016 |
| PAGE: 30 of 97 | |

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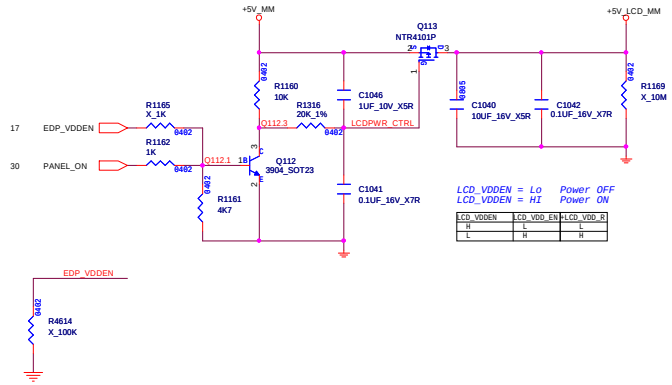
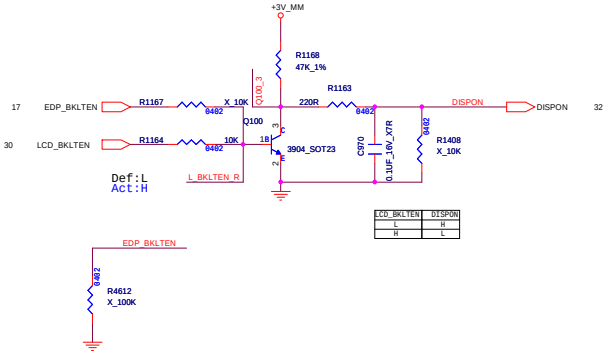
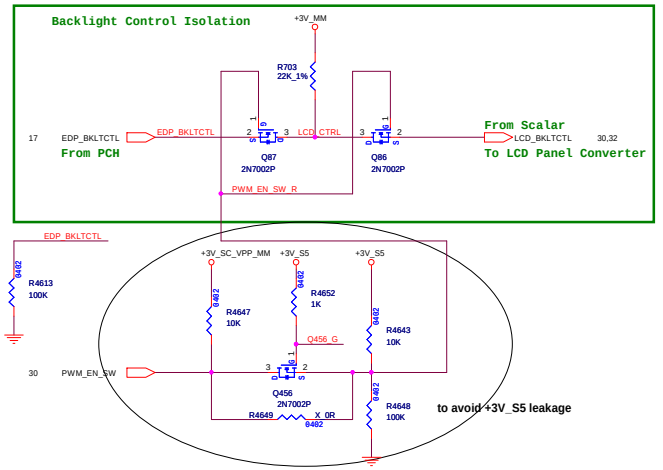
## Panel Controller Power




## Panel Converter Power




## Panel Backlight Control

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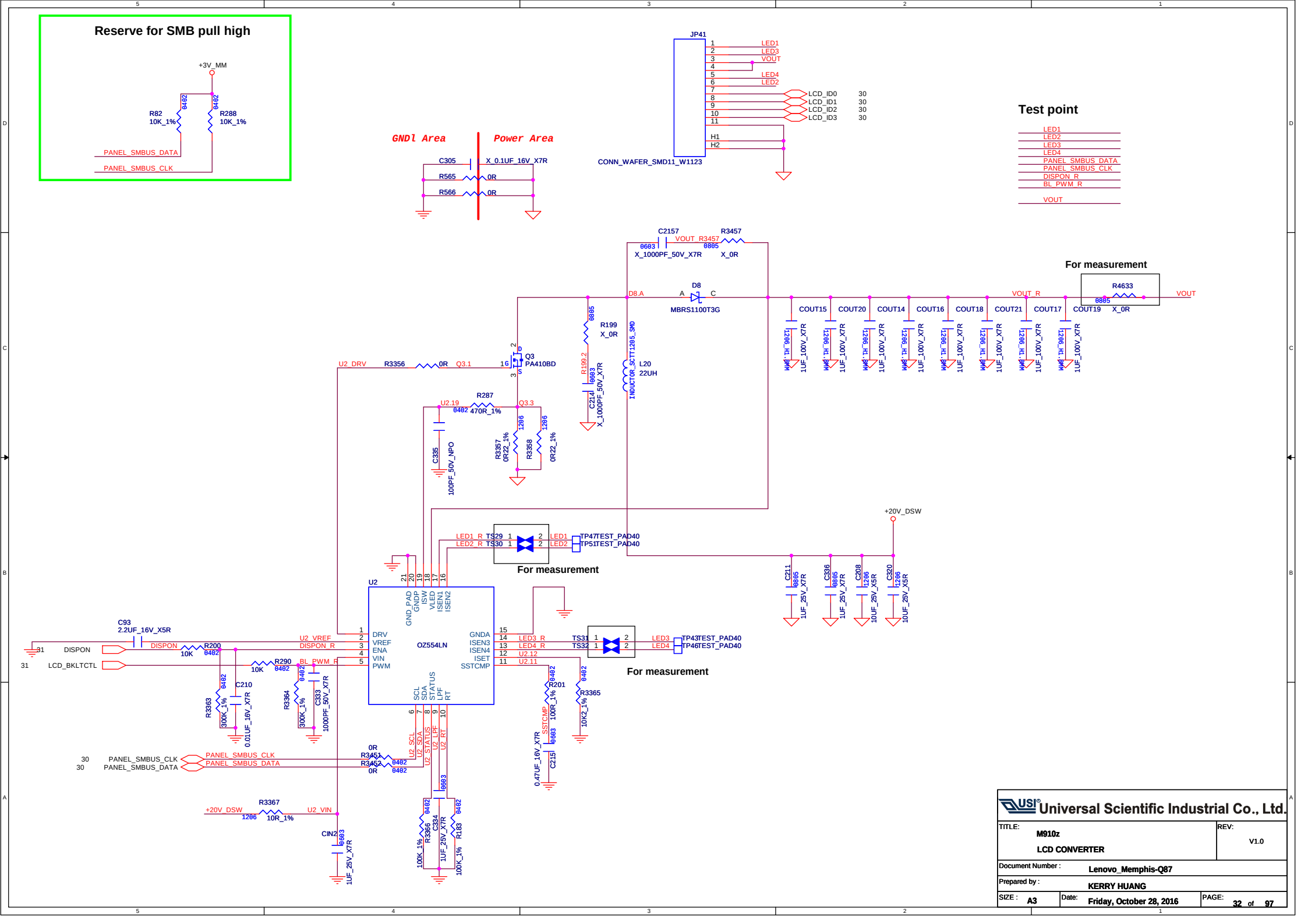
| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M910z LVDS CONN. | REV: V1.0 |
| Document Number : <Doc> | |
| Prepared by : KERRY HUANG | |
| SIZE : A2 | Date: Friday, October 28, 2016 |
| PAGE: 31 of 97 | |

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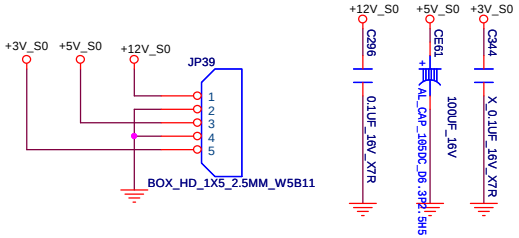
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z LCD CONVERTER | | | REV: V1.0 |
| Document Number : | Lenovo_Memphis-Q87 | | |
| Prepared by : | KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 32 of 97 | |

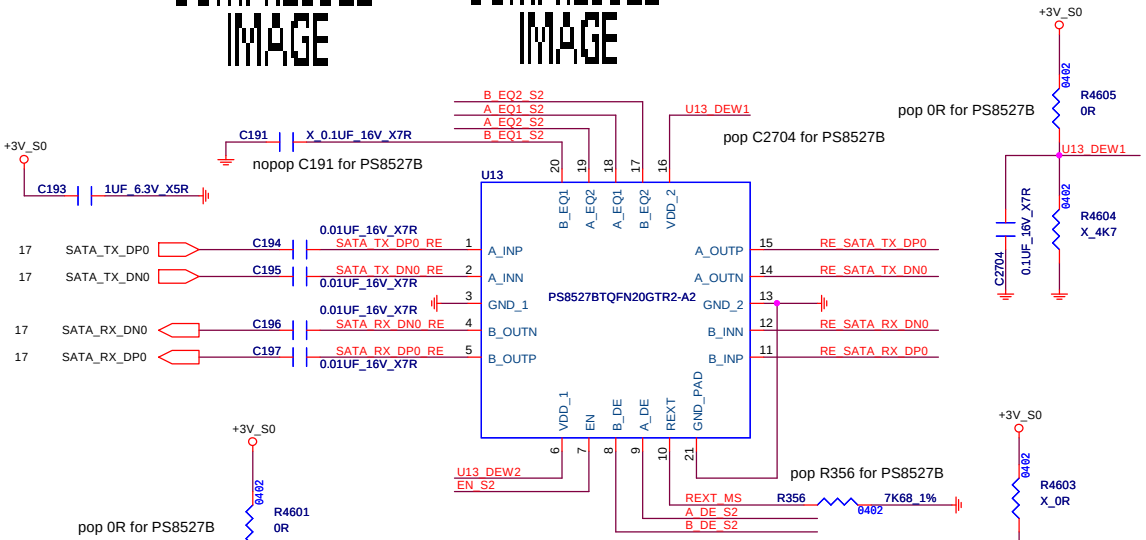
# SATA CONN
## SATA 3.0

COMPRESSED IMAGE

### Power Connector

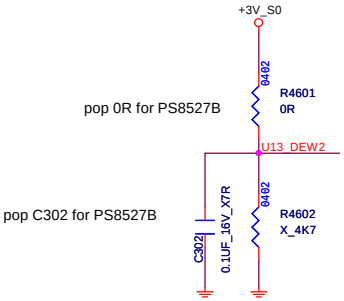


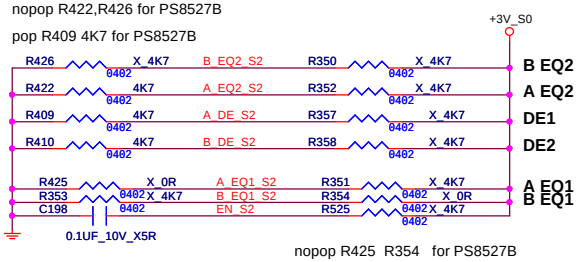

### SATA1 Gen3

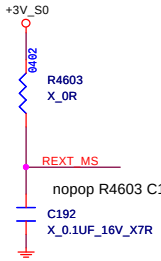




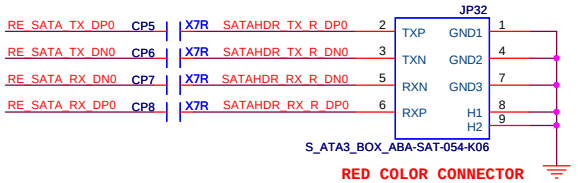




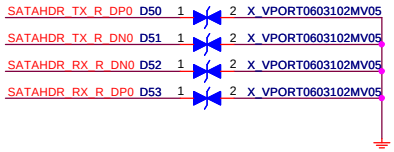




### HDD

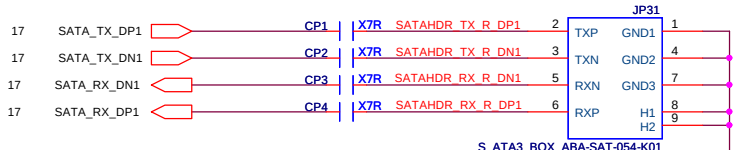



RED COLOR CONNECTOR

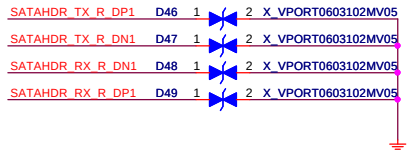



### SATA2 Gen3

### ODD



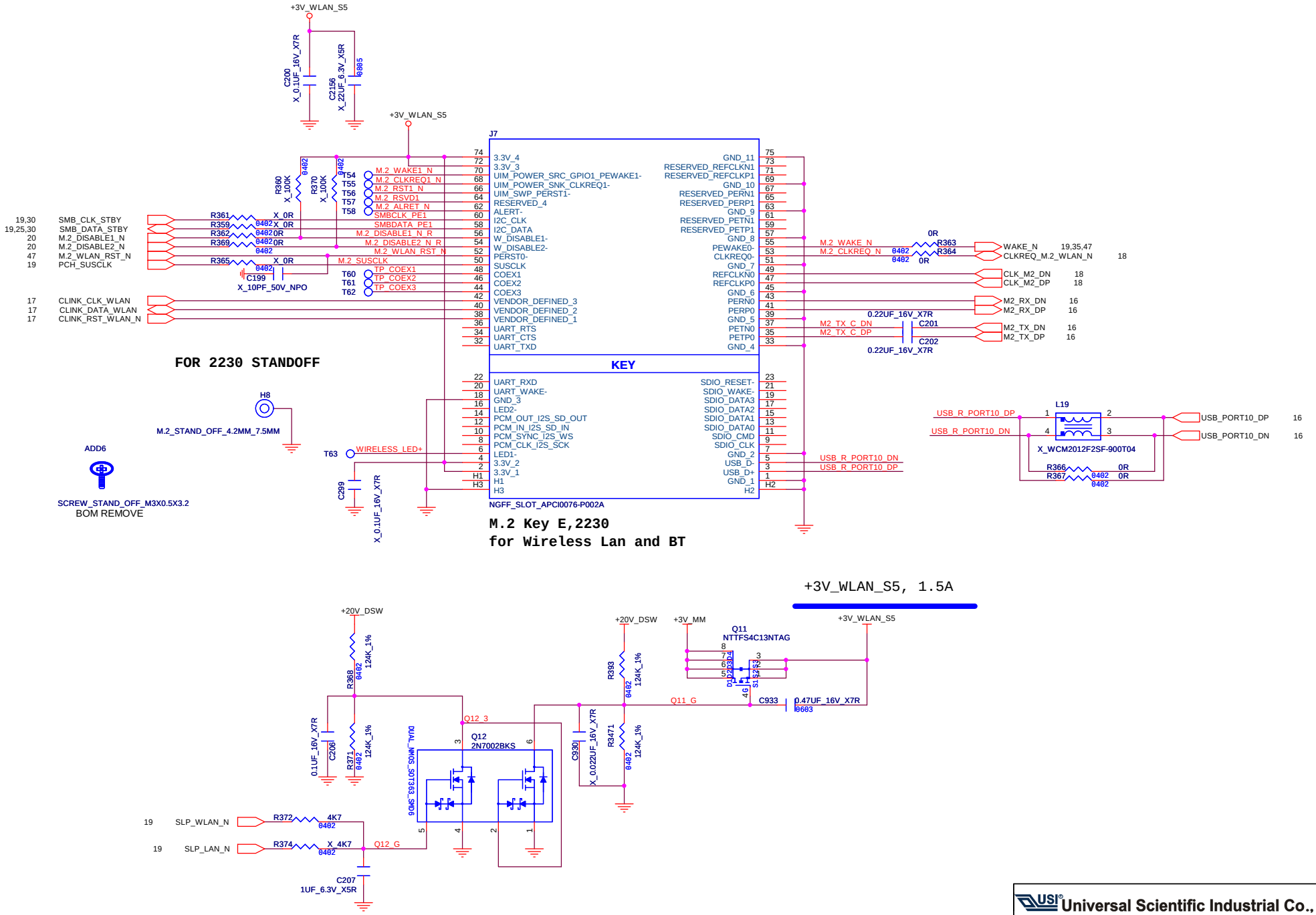

BLACK COLOR CONNECTOR




SN75LVCP601RTJR

COMPRESSED IMAGE

| | | |
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z SATA 3.0 CONN | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 33 of 97 |

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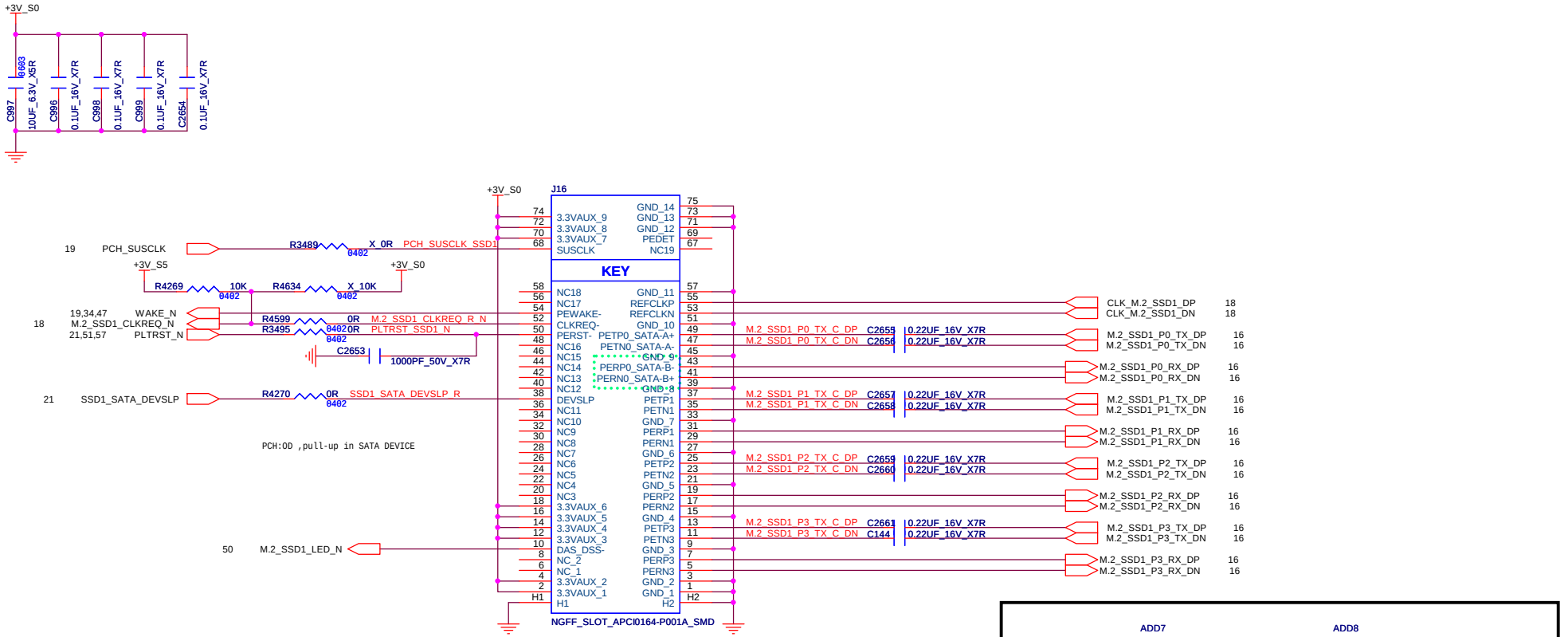
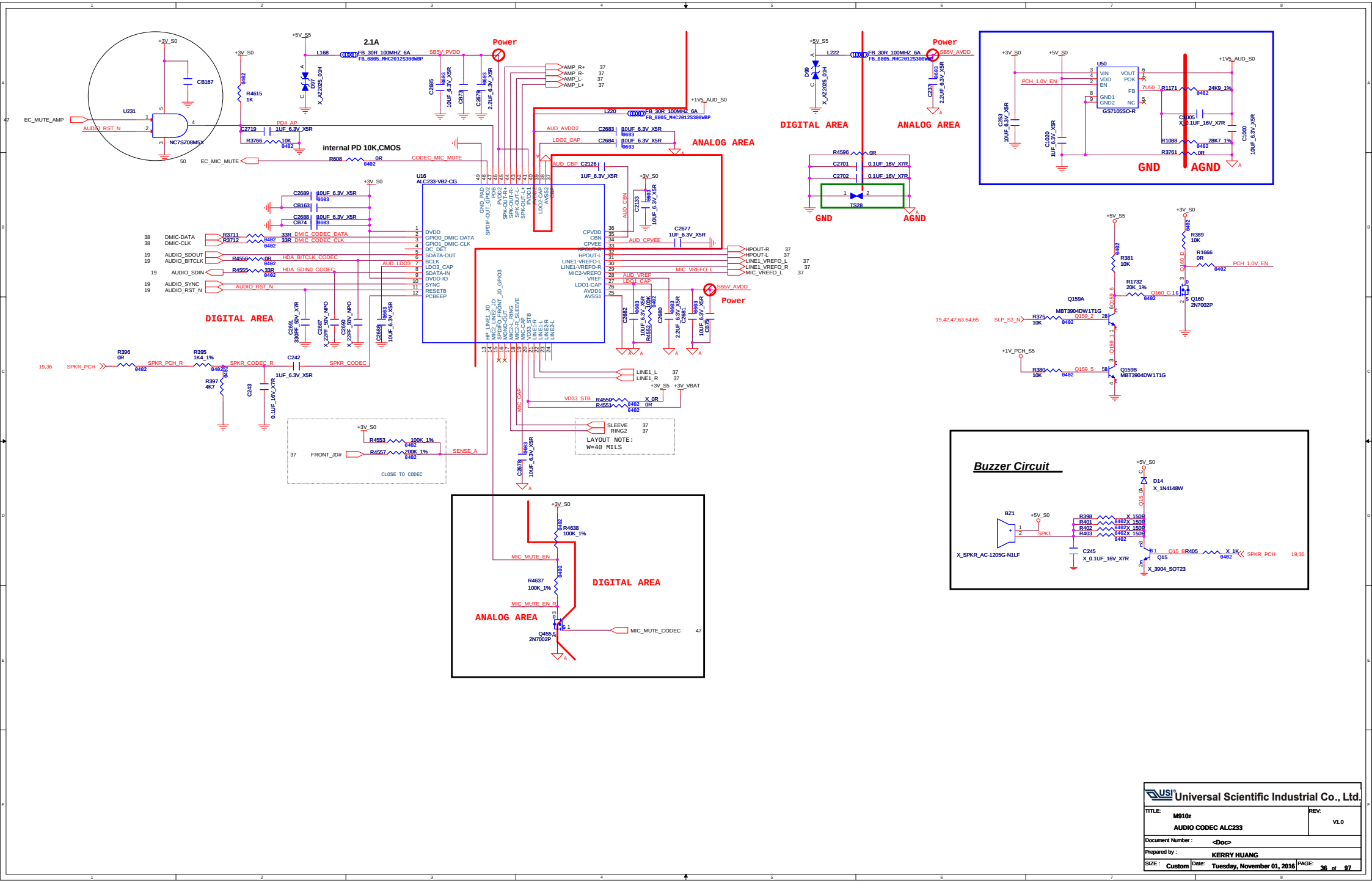
|---|---|
| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M910z<br>M.2 Socket-WLAN | REV: V1.0 |
| Document Number : Lenovo_Motuo | |
| Prepared by : KERRY HUANG | |
| SIZE : A3 | Date: Friday, October 28, 2016 |
| PAGE: 34 of 97 | |




# NGFF KEY M SLOT1 BLACK
# TYPE 2280 H=8.5mm

**NOTE: set 4 X1 from FITC for M.2 RX testing**

| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z<br>M.2 SOCKET-SSD | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 35 of 97 | |


2.1A
Power
internal PD 10K,CMOS
ANALOG AREA
DIGITAL AREA
DIGITAL AREA
ANALOG AREA
GND
AGND
GND
AGND
Power
Power
LAYOUT NOTE:
W=40 MILS
CLOSE TO CODEC
Buzzer Circuit
DIGITAL AREA
ANALOG AREA
Universal Scientific Industrial Co., Ltd.
M910z
AUDIO CODEC ALC233
V1.0
<Doc>
KERRY HUANG
Custom
Tuesday, November 01, 2016
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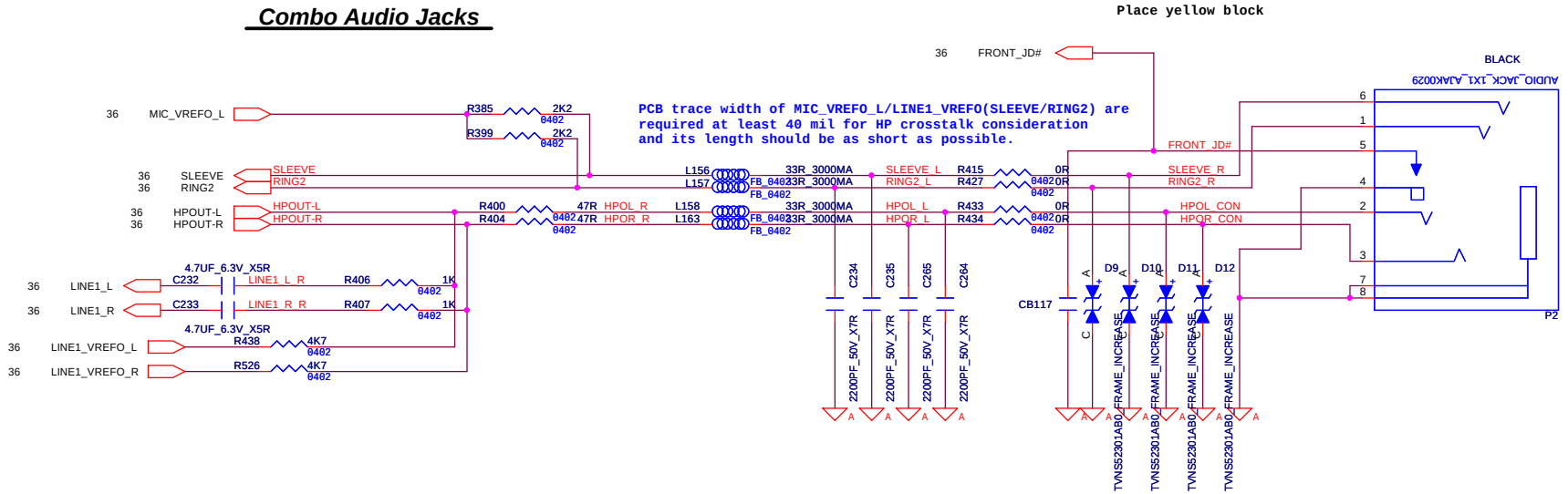
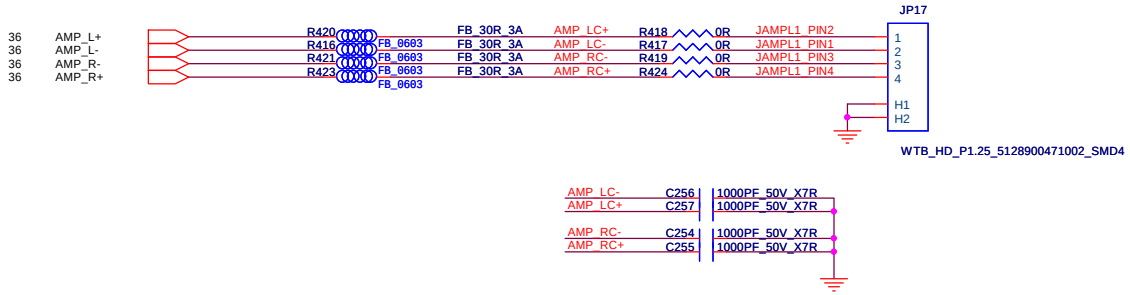
# Combo Audio Jacks




## SPEAKER

**4Ω +-15%**
**Rated Power :3W**
**Max. Power:5W**

**Required at least 40 mil**

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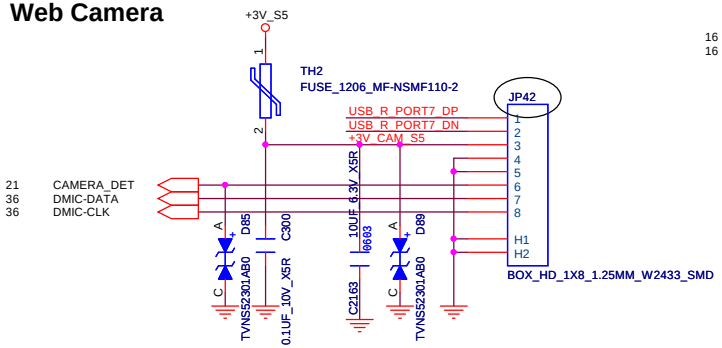
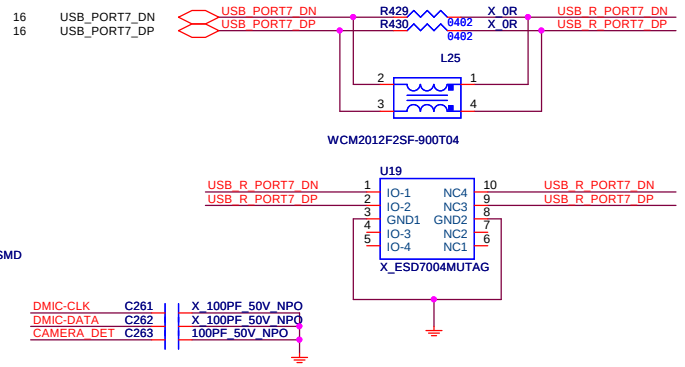
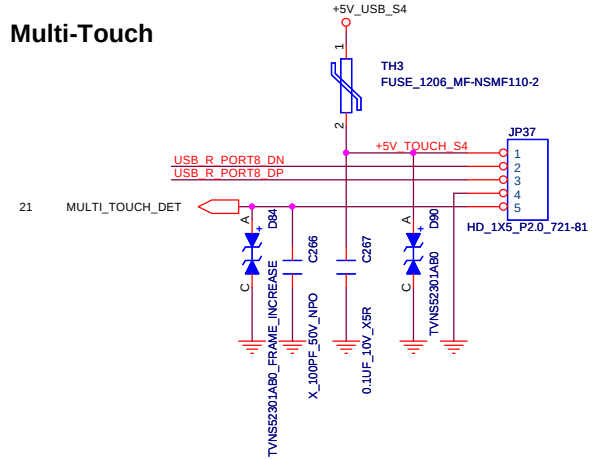
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z AUDIO JACK | | | REV: V1.0 |
| Document Number : Lenovo_Memphis-Q87 | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 37 of 97 |

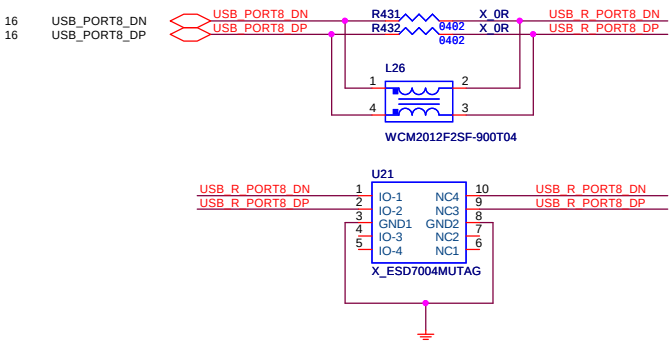
## Web Camera



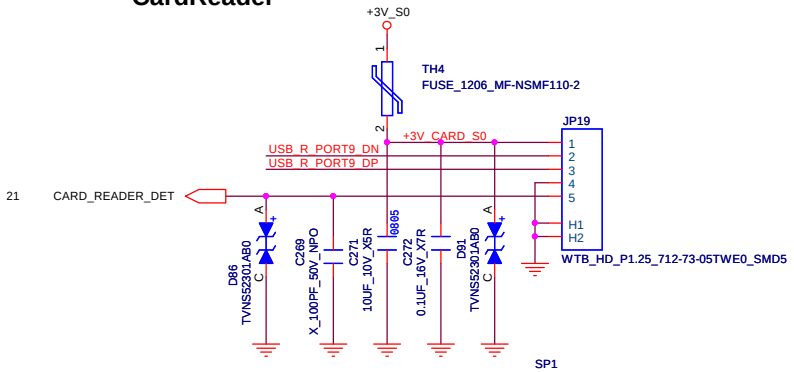



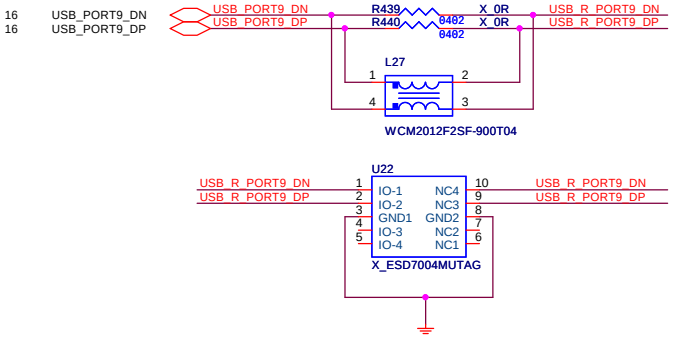

## Multi-Touch

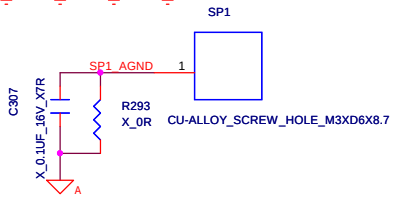



## CardReader

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| | | | |
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| TITLE: M910z USB 2.0 (3PORT) | | | REV: V1.0 |
| Document Number : | Lenovo_Memphis-Q87 | | |
| Prepared by : | KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: | 38 of 97 |

ADD9

STAND_OFF_M2X0.4XL5.8

H42

SCREW_HOLE_PTH_2.3MM_4.5MM

16 USB_PORT11_DN
16 USB_PORT11_DP
R4292 0R 0402 USB_PORT11_CONN_DN
R4293 0R 0402 USB_PORT11_CONN_DP
L165
X_WCM2012F2SF-900T04

16 USB3_RXN7
16 USB3_RXP7
R4291 0R 0402
R4290 0R 0402
USB3_RXN7_CON
USB3_RXP7_CON
L68
X_WCM2012F2SF-900T04

16 USB3_TXN7
16 USB3_TXP7
R4288 0R 0402
R4289 0R 0402
USB3_TXN7_CON
USB3_TXP7_CON
L164
X_WCM2012F2SF-900T04

D101
USB3_TXN7_CON
USB3_TXP7_CON
USB3_RXN7_CON
USB3_RXP7_CON
IN1 IN2 GND IN3 IN4 NC1 NC2 NC3 NC4 GND
X_TVWDF1004AD0

D102
USB_PORT11_CONN_DN
USB_PORT11_CONN_DP
TVWDF1004AD0

+5V_USB_S4

Power

C2694 22UF_6.3V_X5R 0805

D96 X_TVNS52301AB0

CM4

C2671 0603 1000PF_50V_X7R

JP36
USB_PORT11_CONN_DP
USB_PORT11_CONN_DN
USB3_RXP7_CON
USB3_RXN7_CON
USB3_TXP7_CON
USB3_TXN7_CON
H1
H2
USB_TYPEC_HD_P0.5_SMD12_88511

20 PO_USB3.0_PRES_N
R4294 1K5 0402
PO_USB3.0_PRES_R_N

D95 X_TVNS52301AB0

C2672 0603 1000PF_50V_X7R

+5V_USB_S4

R3566 10K 0402

16 USB_OC_PORT7_N

C1145 1000PF_50V_X7R

R3565 15K 0402

D103 X_TVNS52301AB0

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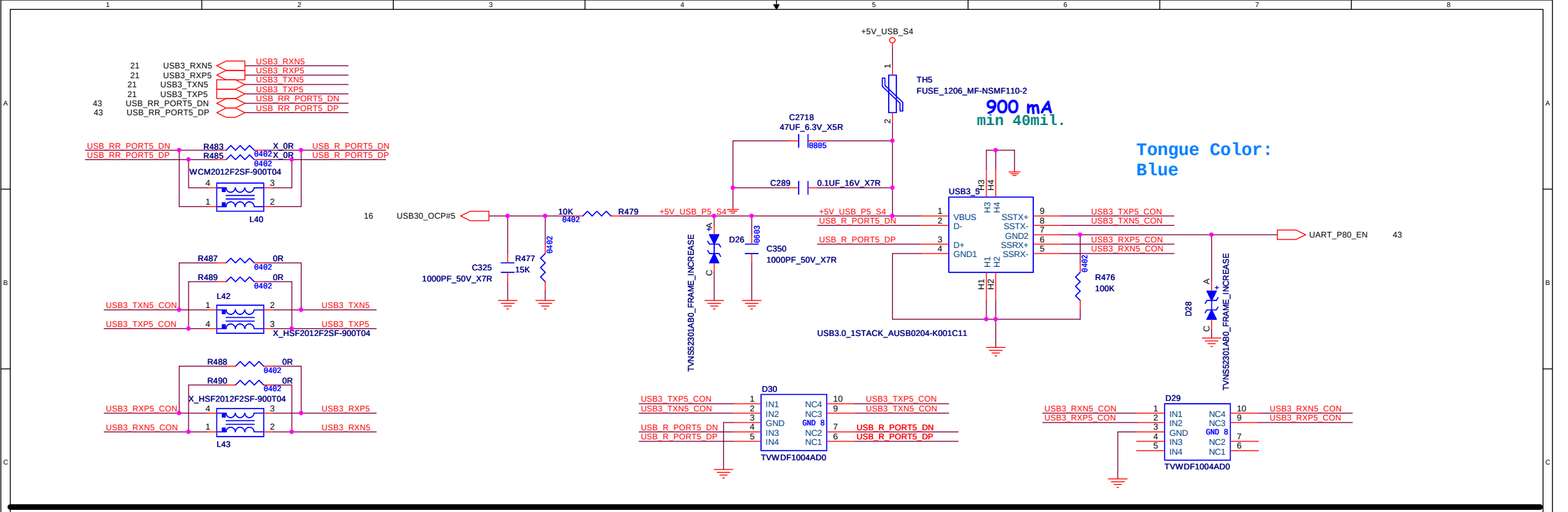
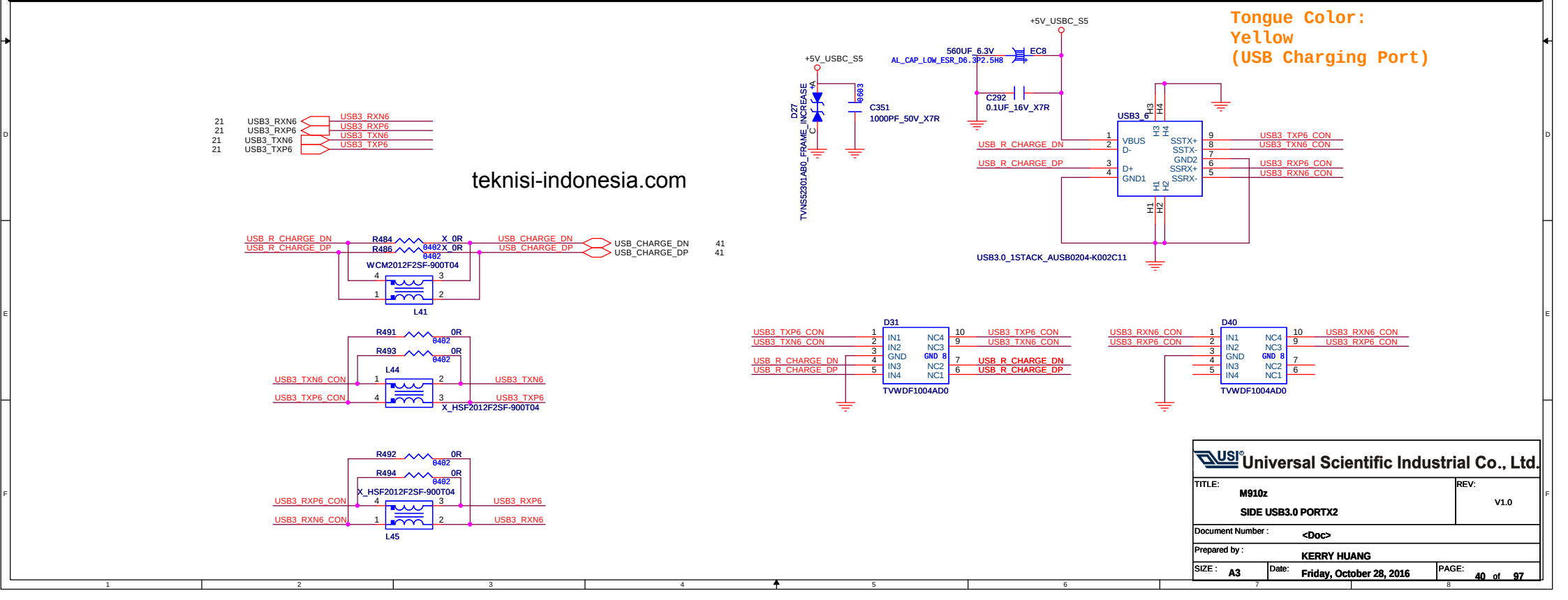
|---|---|---|---|
| USI® Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Tuesday, November 01, 2016 | | PAGE: 39 of 97 |

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| | |
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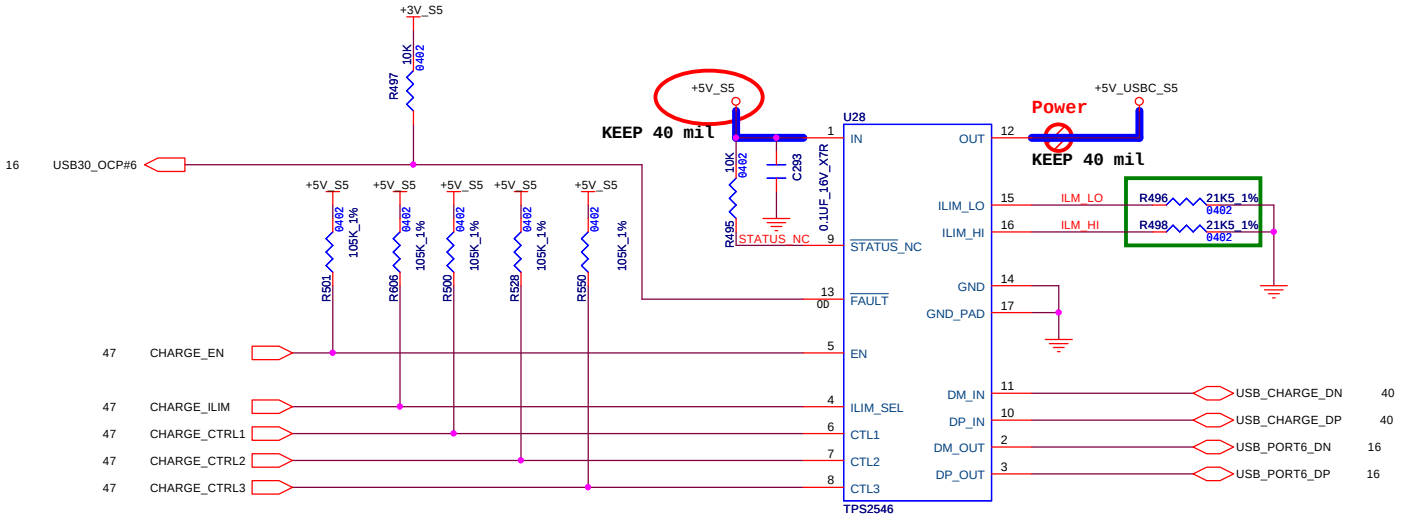
| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M910z SIDE USB3.0 PORTX2 | REV: V1.0 |
| Document Number : <Doc> | |
| Prepared by : KERRY HUANG | |
| SIZE : A3 | Date: Friday, October 28, 2016 |
| PAGE: 40 of 97 | |

# USB CHARGING PORT CONTROLLER & POWER SWITCH WITH LOAD DETECTION



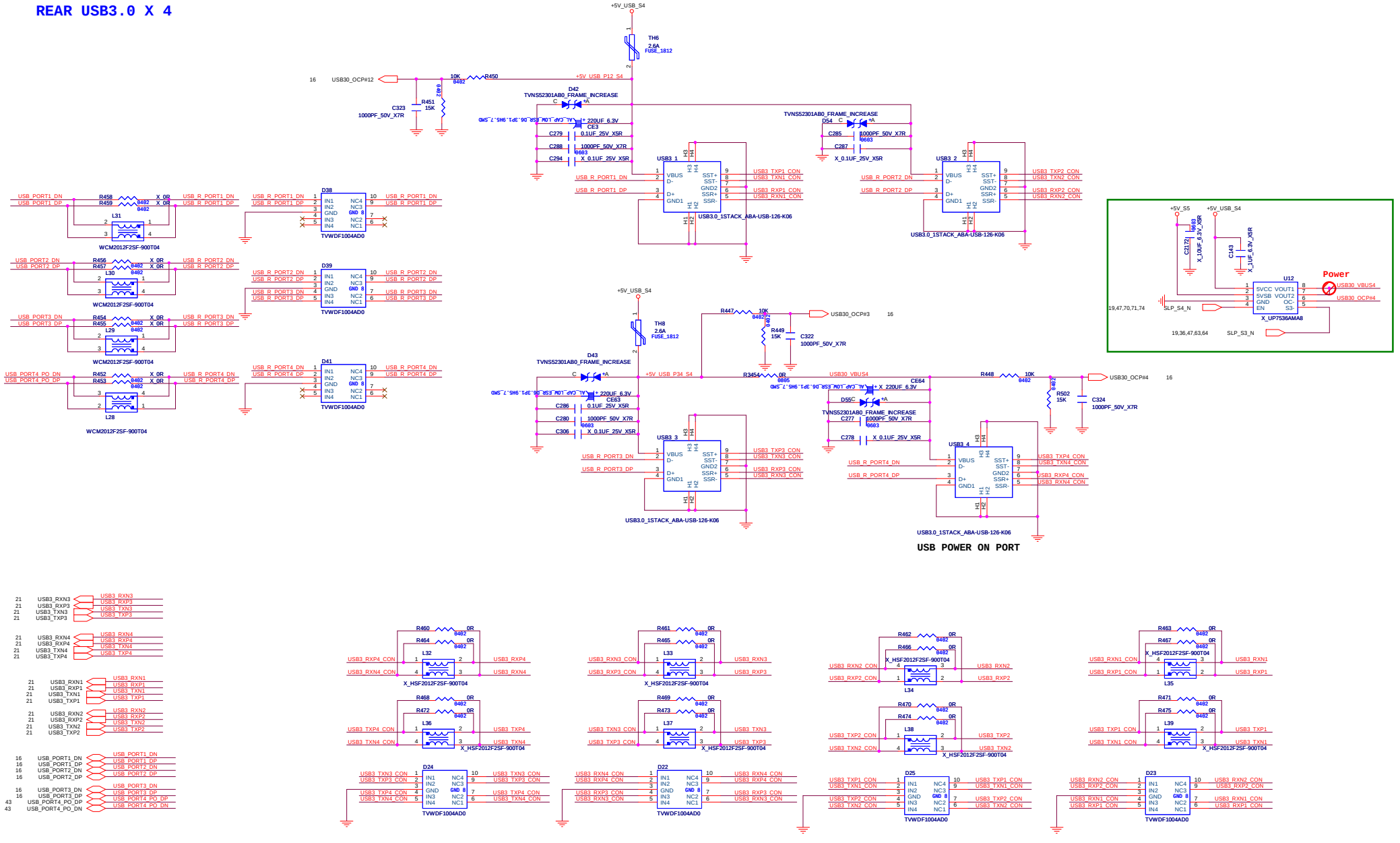

A :TPS2546RTET
B :NCT3955Y
C :PI5USB2546ZHEX

| Control Signal | | | Model Select | | | | |
|---|---|---|---|---|---|---|---|
| | | | CNTL1 | CNTL2 | CNTL3 | ILIM_SEL | EN |
| Charge EN | S0 | CDP | 1 | 1 | 1 | 1 -ILIM_HI | 1 |
| | S3 | DCP | 0 | 1 | 1 | 0 -ILIM_HI | 1 |
| | S4/S5 | DCP | 0 | 0 | 1 | 1 -ILIM_HI | 1 |
| Charge DIS | S0 | SDP | 0 | 1 | 0 | 0 -ILIM_LO | 1 |
| | S3 | SDP | 0 | 1 | 0 | 0 -ILIM_LO | 1 |
| | S4/S5 | SDP | Shunt Down | | | | 0 |
| Logic | | | AND (EN_GPIO,SLP_S3#) | AND (OR(EN_GPIO#,MODE),SLP_S4#) | EN_GPIO | AND (SLP_S3#, SLP_S4) | OR (EN_GPIO,SLP_S4#) |

Universal Scientific Industrial Co., Ltd.

| | | | |
|---|---|---|---|
| TITLE: M910z USB CHARGING | | | REV: V1.0 |
| Document Number : | Lenovo_Memphis-Q87 | | |
| Prepared by : | KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 41 of 97 |

# REAR USB3.0 X 4

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| Universal Scientific Industrial Co., Ltd. | | |
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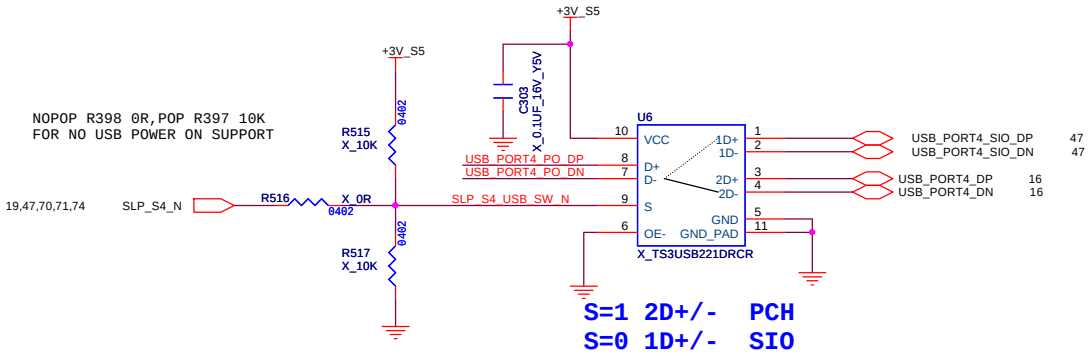
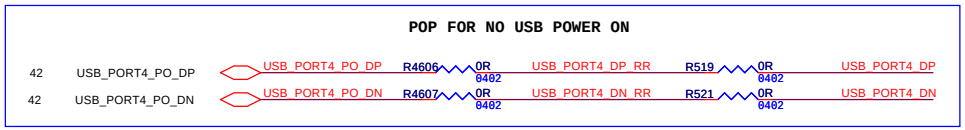
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A2 | Date: Friday, October 28, 2016 | PAGE: 42 of 97 |

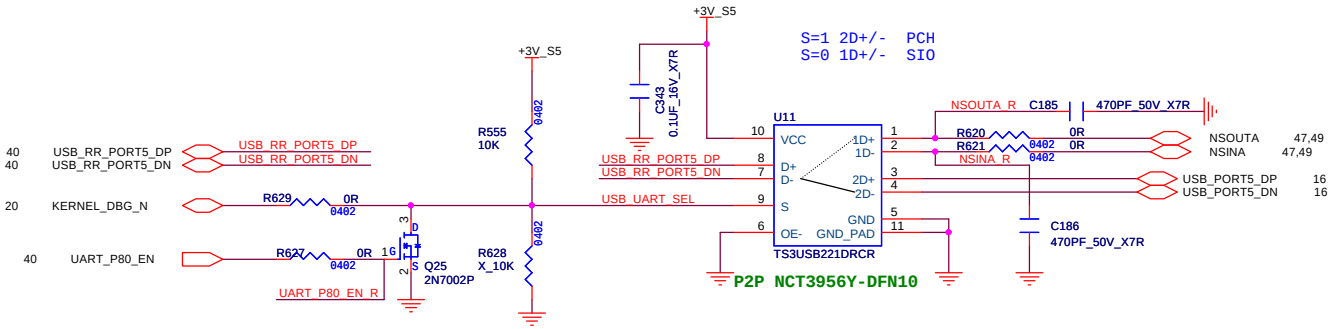
# USB POWER ON RESERVE




| OE# | S | Funtion |
|---|---|---|
| H | X | Disable |
| L | L | D(+/-) to 1D(+/-) |
| L | H (Default) | D(+/-) to 2D(+/-) |




# USB Debug




| PCH_GPIO_D16 | kernel debug |
|---|---|
| Set input | DISABLE |
| Set output Low | ENABLE |

| UARTA_P80_EN | POST 80 |
|---|---|
| L | DISABLE |
| H | ENABLE |

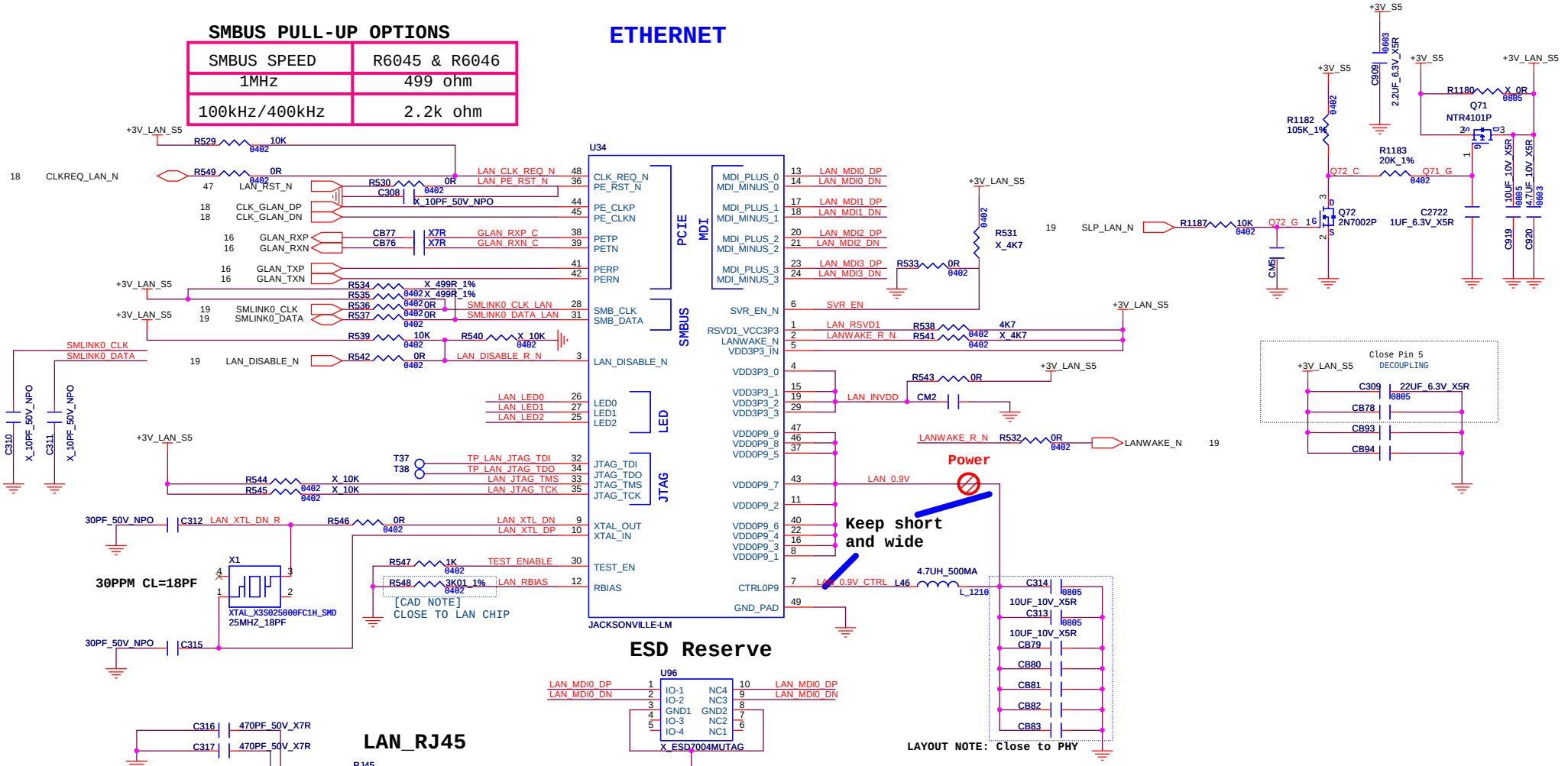
Universal Scientific Industrial Co., Ltd.

| | |
|---|---|
| TITLE: M910z<br>USB POWER ON/Debug | REV: V1.0 |
| Document Number : <Doc> | |
| Prepared by : KERRY HUANG | |
| SIZE : A3 | Date: Friday, October 28, 2016 |
| PAGE: 43 of 97 | |

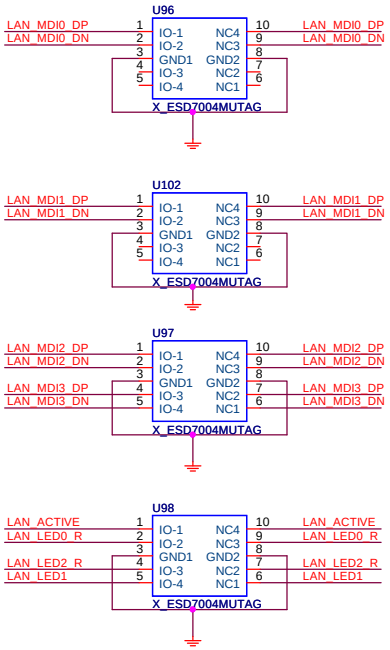
# ETHERNET

## SMBUS PULL-UP OPTIONS

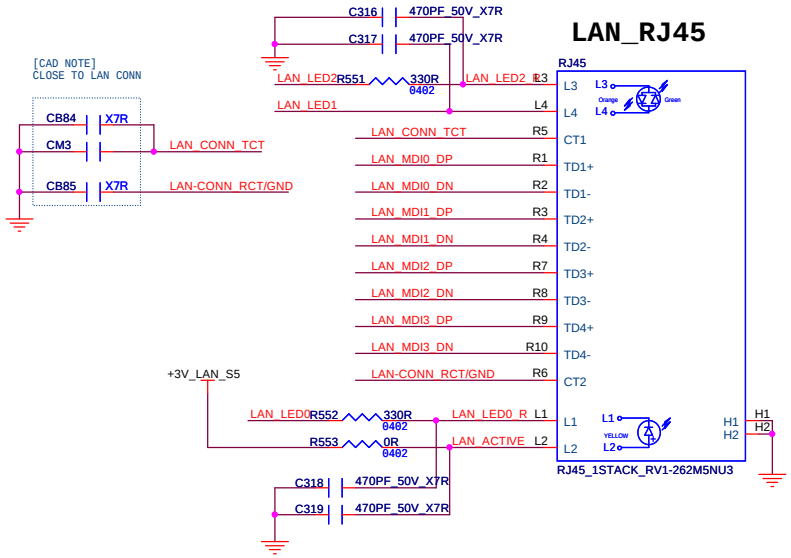
| SMBUS SPEED | R6045 & R6046 |
|---|---|
| 1MHz | 499 ohm |
| 100kHz/400kHz | 2.2k ohm |



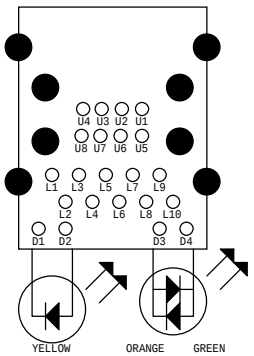

## ESD Reserve




## LAN_RJ45




LAYOUT NOTE: Close to PHY

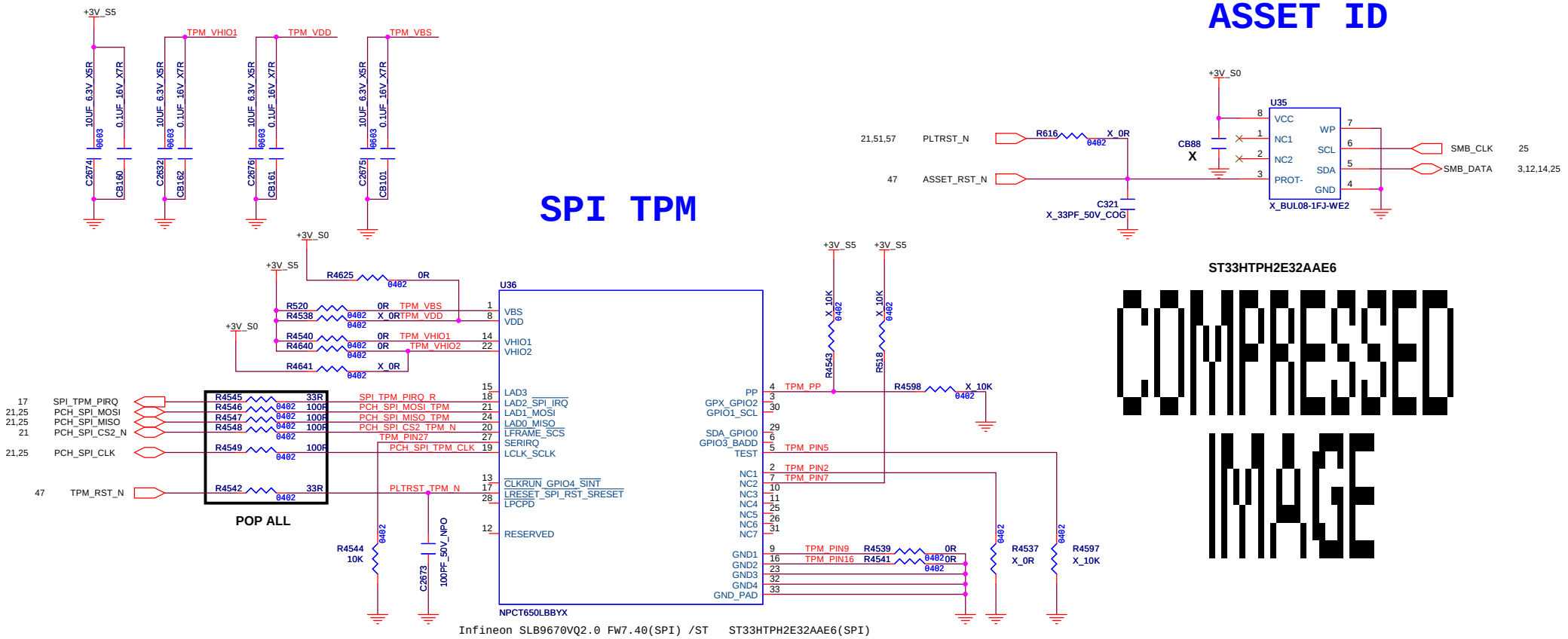



| WOL | Status | Yellow | Green | Orange |
|---|---|---|---|---|
| Don't care | No Link | | | |
| Off | S3/S4/S5 | | | |
| On | 10Mb Inactive | | | |
| On | 10Mb Active | B | | |
| On | 100Mb Inactive | | | |
| On | 100Mb Active | B | | |
| On | 1Gb Inactive | | | |
| On | 1Gb Active | B | | |

Universal Scientific Industrial Co., Ltd.

| | | |
|---|---|---|
| TITLE: M910z LAN JACKSONVILLE | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 44 of 97 |

# SPI TPM




Infineon SLB9670VQ2.0 FW7.40(SPI) /ST ST33HTPH2E32AAE6(SPI)

# ASSET ID




ST33HTPH2E32AAE6

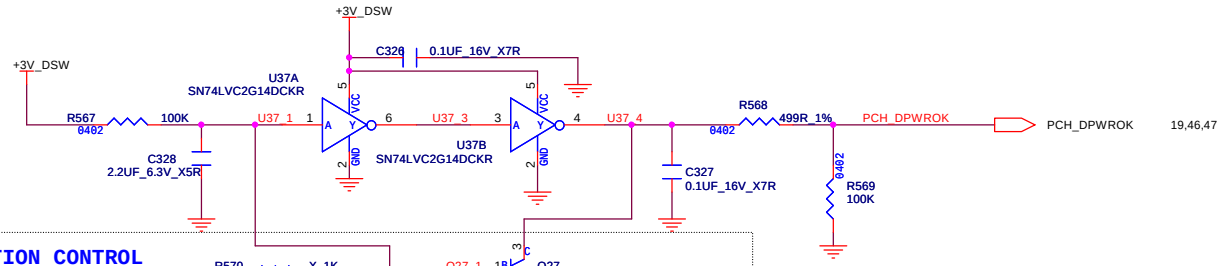
COMPRESSED IMAGE

| | STUFF | EMPTY |
|---|---|---|
| **NPCT650LBBYX** | R520,R4538,R4540 | R518,R4543,R4537,R4597,R4598 |
| ST33HTPH2E32AAE6 | R4537 | R520,R4543,R518,R4538,R4539,R4540,R4541,R4544 ,C2632,CB162,C2676,CB161,C2675,CB101,R4597,R4598 |
| SLB9670V | R520,R4539,R4537 | R518,R4543,R4544,R4597,R4598 |

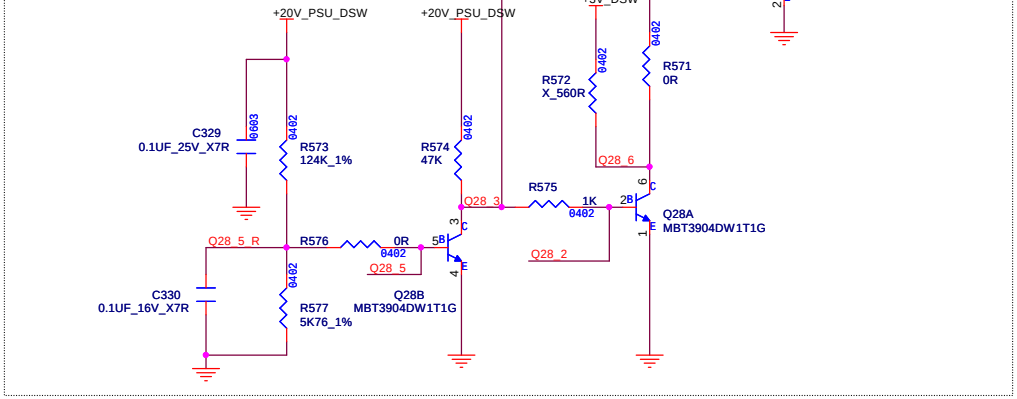
Universal Scientific Industrial Co., Ltd.

| | | |
|---|---|---|
| TITLE: M910z TPM_ASSET ID | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 45 of 97 |

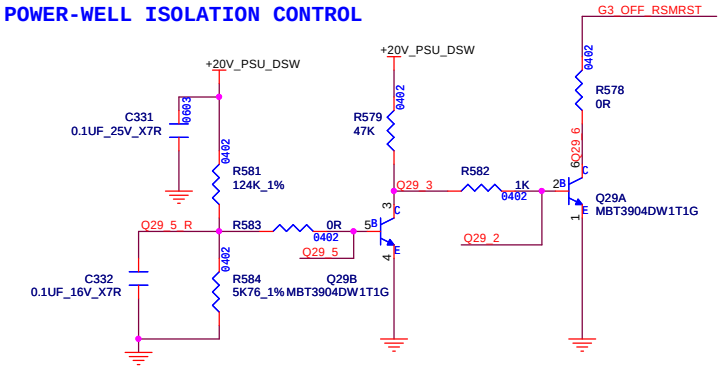
# DPWROK LOGIC

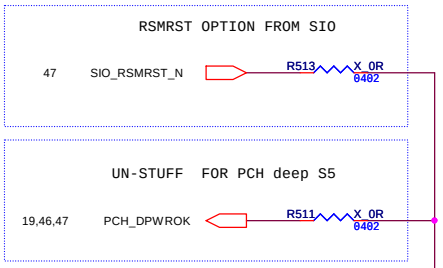


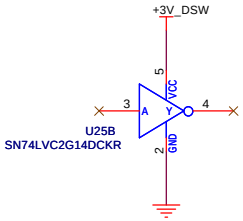

## POWER-WELL ISOLATION CONTROL



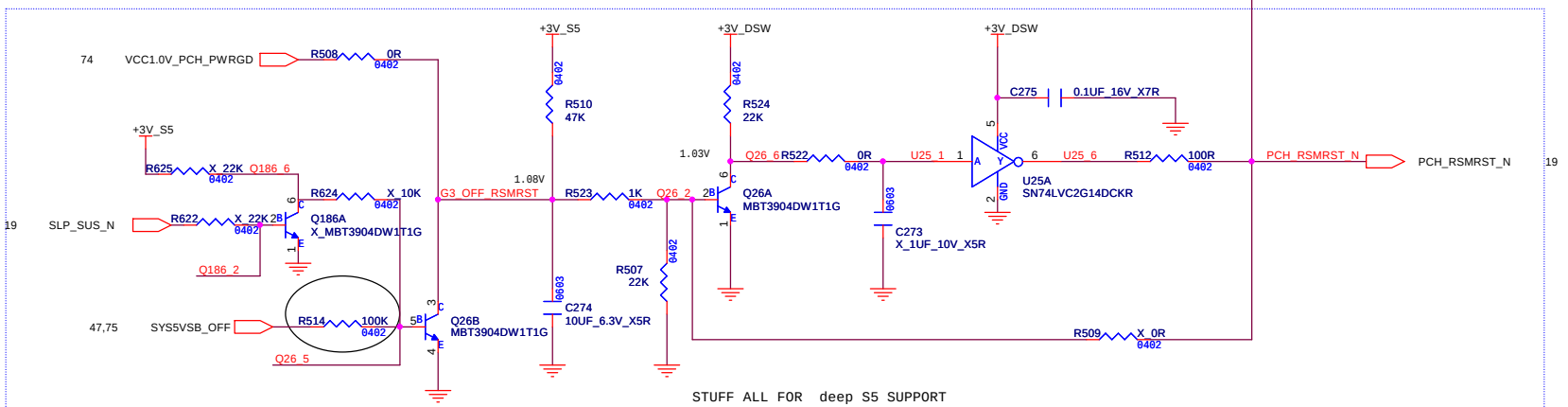

## POWER-WELL ISOLATION CONTROL




# RSMRST LOGIC

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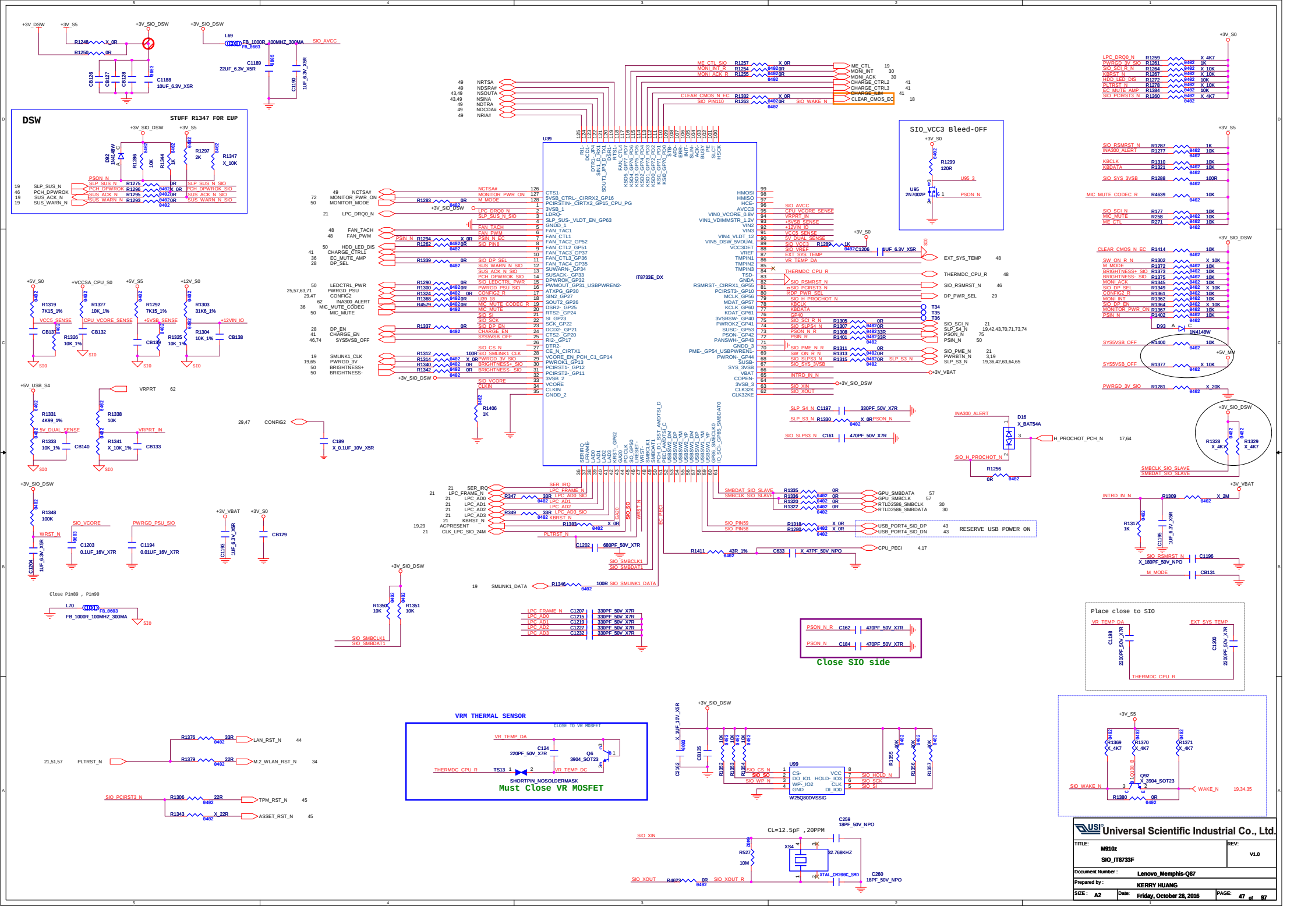
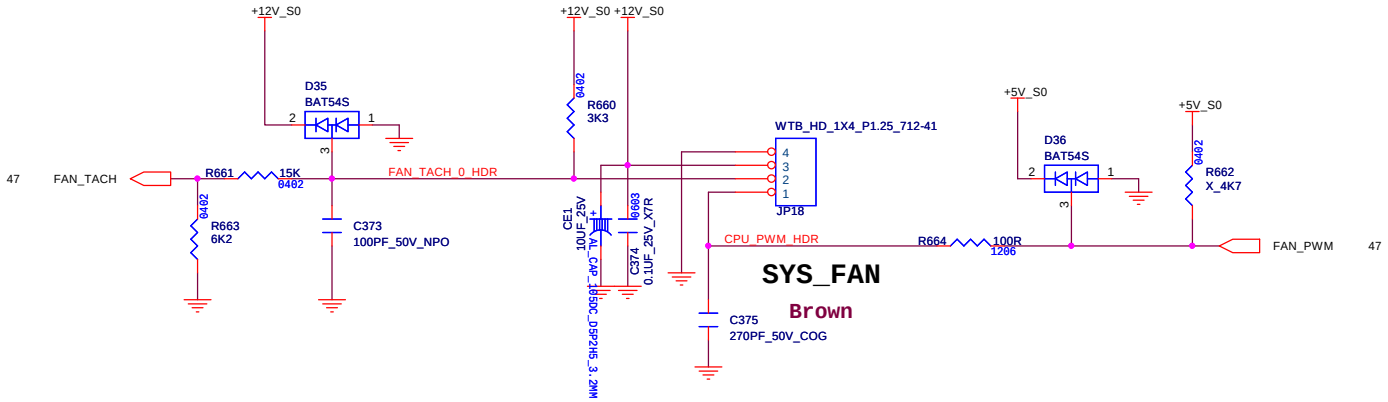
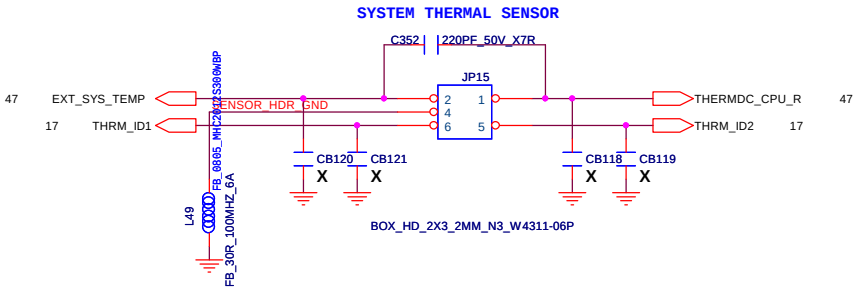
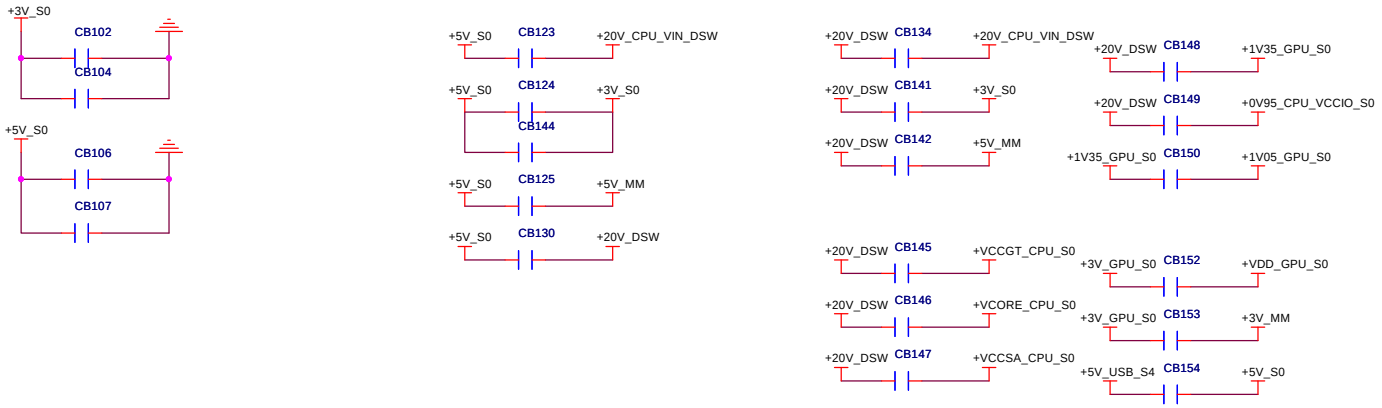
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z RSMRST LOGIC | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 46 of 97 |


DSW
STUFF R1347 FOR EUP
U39
IT8733E_DX
SIO_VCC3 Bleed-OFF
U95
2N7002P
Place close to SIO
Close SIO side
VRM THERMAL SENSOR
CLOSE TO VR MOSFET
SHORTPIN_NOSOLDERMASK
Must Close VR MOSFET
W25Q80DVSSIG
CL=12.5pF ,20PPM
32.768KHZ
RESERVE USB POWER ON
Universal Scientific Industrial Co., Ltd.
TITLE: M910z
SIO_IT8733F
REV: V1.0
Document Number : Lenovo_Memphis-Q87
Prepared by : KERRY HUANG
SIZE : A2
Date: Friday, October 28, 2016
PAGE: 47 of 97

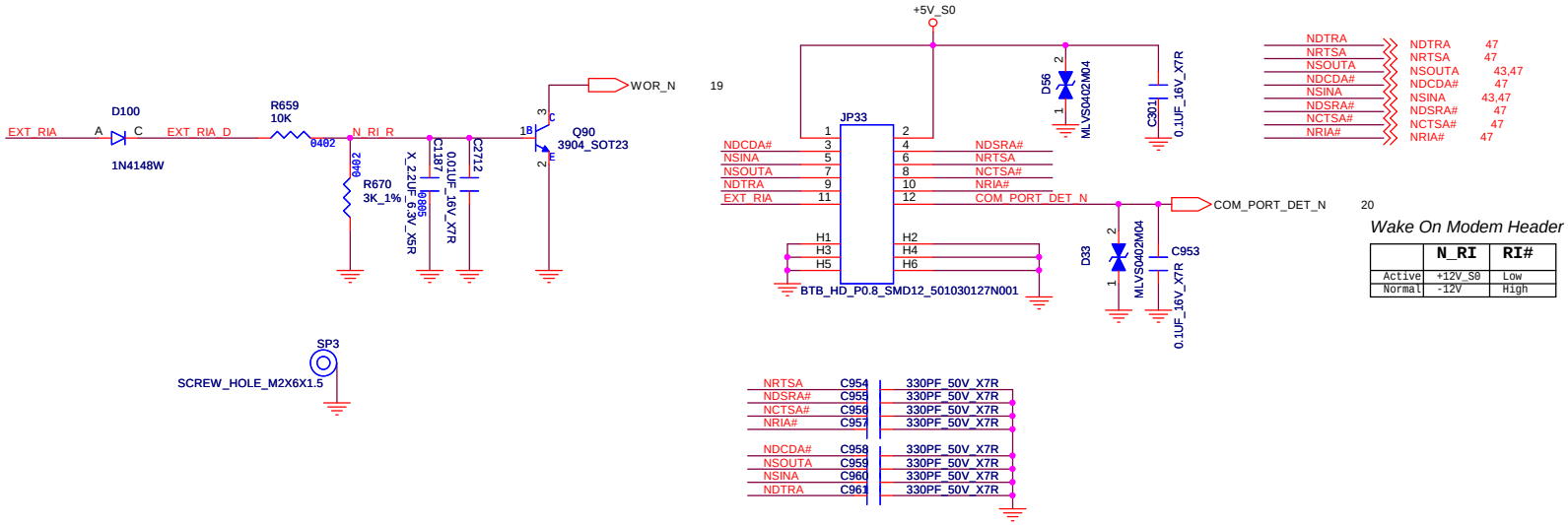



| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z THERMAL_FAN | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 48 of 97 | |

# SERIAL PORT 1

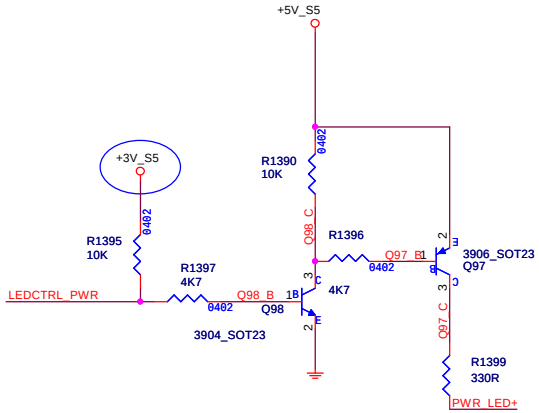



*Wake On Modem Header*

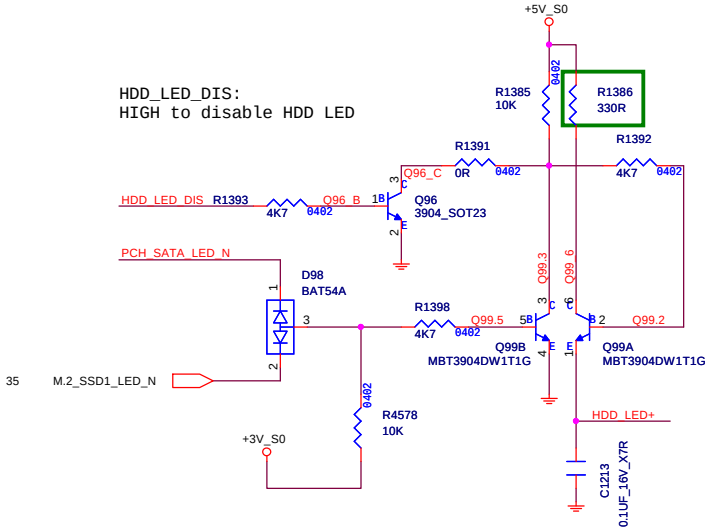
| | N_RI | RI# |
|---|---|---|
| Active | +12V_S0 | Low |
| Normal | -12V | High |

| | |
|---|---|
| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M910z COM | REV: V1.0 |
| Document Number : <Doc> | |
| Prepared by : KERRY HUANG | |
| SIZE : A3 | Date: Friday, October 28, 2016 |
| PAGE: 49 of 97 | |

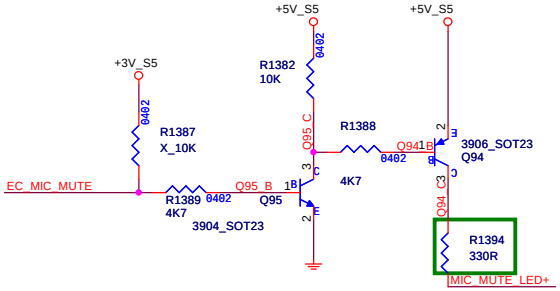
## Power LED




## HDD LED



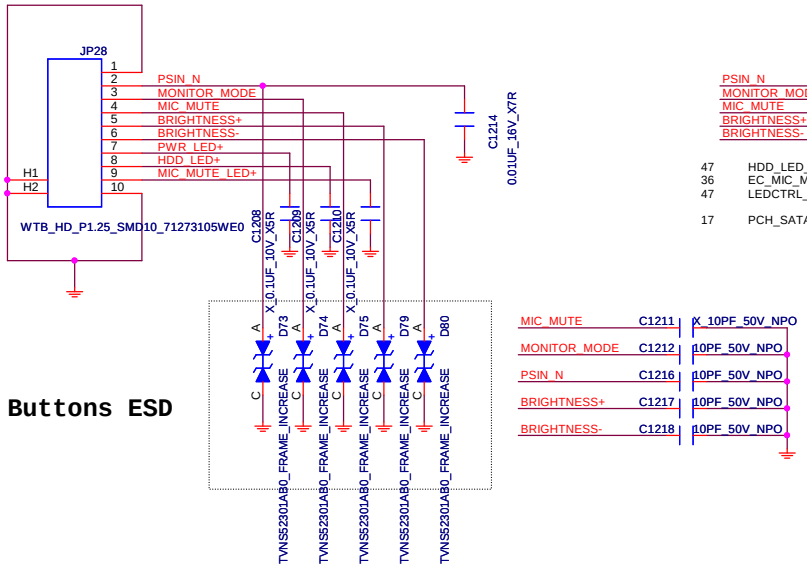

## MIC MUTE LED




**Max power consumption on R1386,R1394,R1399 are 0.025W**

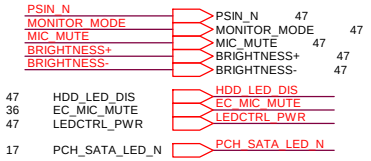
| State | LED Behavior |
|---|---|
| Power On | LED On |
| Standby | Blinking |
| Power Off | LED Off |

## Front Switch Button/LED

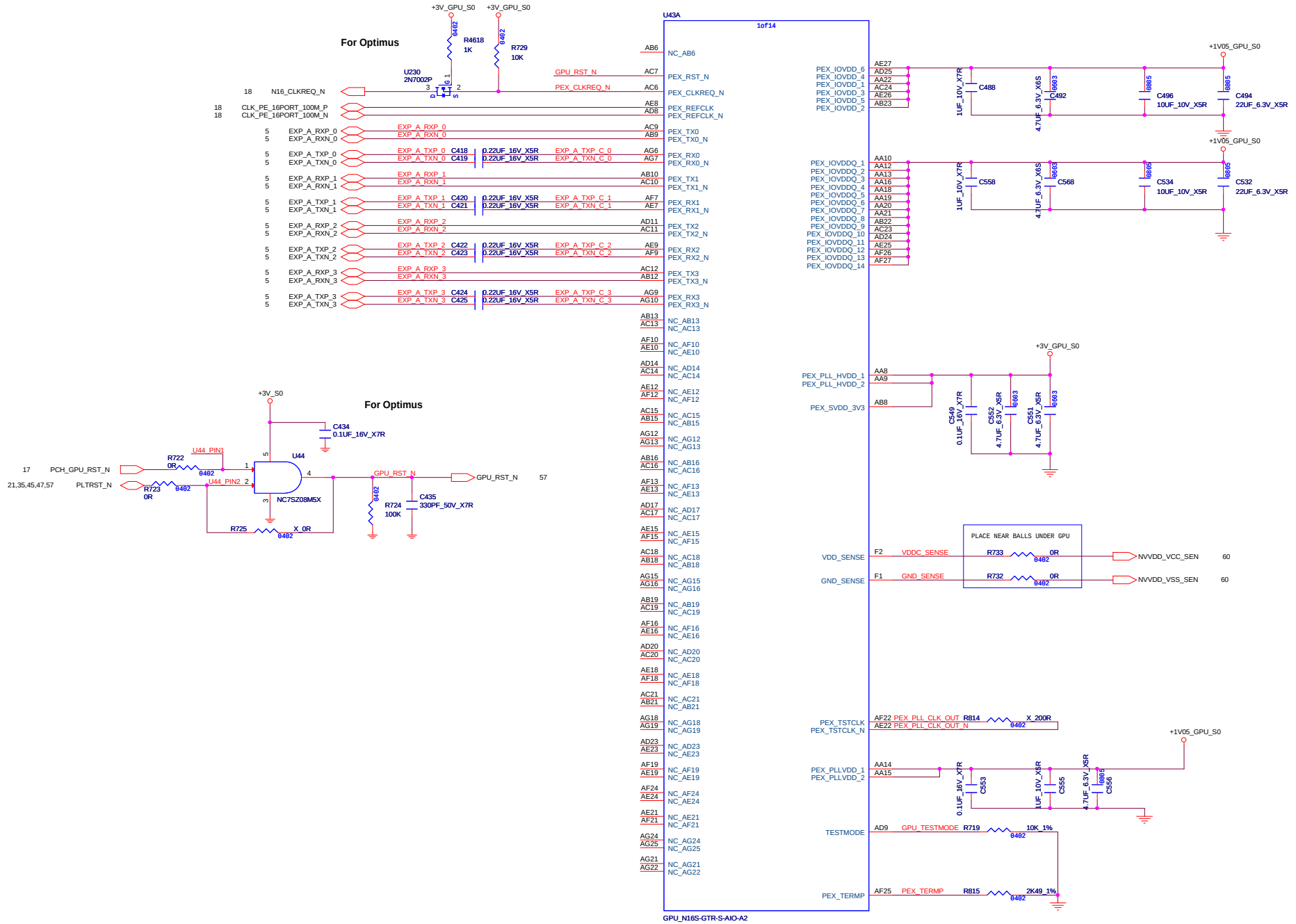



**Buttons ESD**

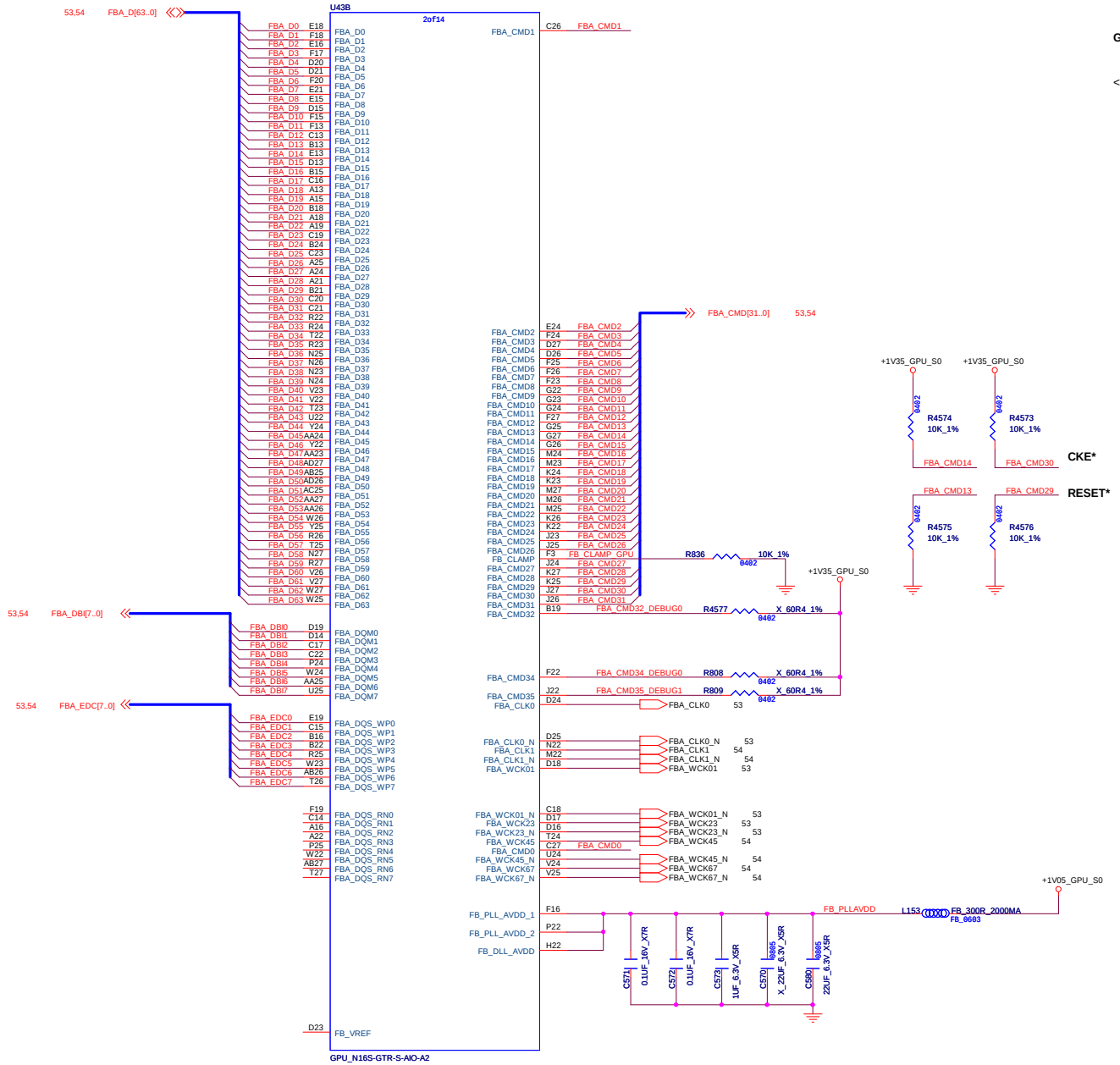



| | | |
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z FUNCTION BUTTON | | REV: V1.0 |
| Document Number : Lenovo_Memphis-Q87 | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 50 of 97 |




| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z N16S_PCIE | | | REV: V1.0 |
| Document Number : Lenovo_Memphis-Q87 | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : Custom | Date: Friday, October 28, 2016 | | PAGE: 51 of 97 |




**GDDR5 CMD MAPPING TABLE**

| <0..31> | <32..63> | MEMORY |
|---|---|---|
| 12 | 28 | RAS |
| 15 | 31 | CAS |
| 5 | 21 | WE |
| 0 | 16 | CS |
| 8 | 24 | ABI |
| 10 | 26 | A0_A10 |
| 11 | 27 | A1_A9 |
| 2 | 18 | A2_BA0 |
| 1 | 17 | A3_BA3 |
| 3 | 19 | A4_BA2 |
| 4 | 20 | A5_BA1 |
| 7 | 23 | A6_A11 |
| 6 | 22 | A7_A8 |
| 9 | 25 | A12_RFU |
| 14 | 30 | CKE |
| 13 | 29 | RESET |

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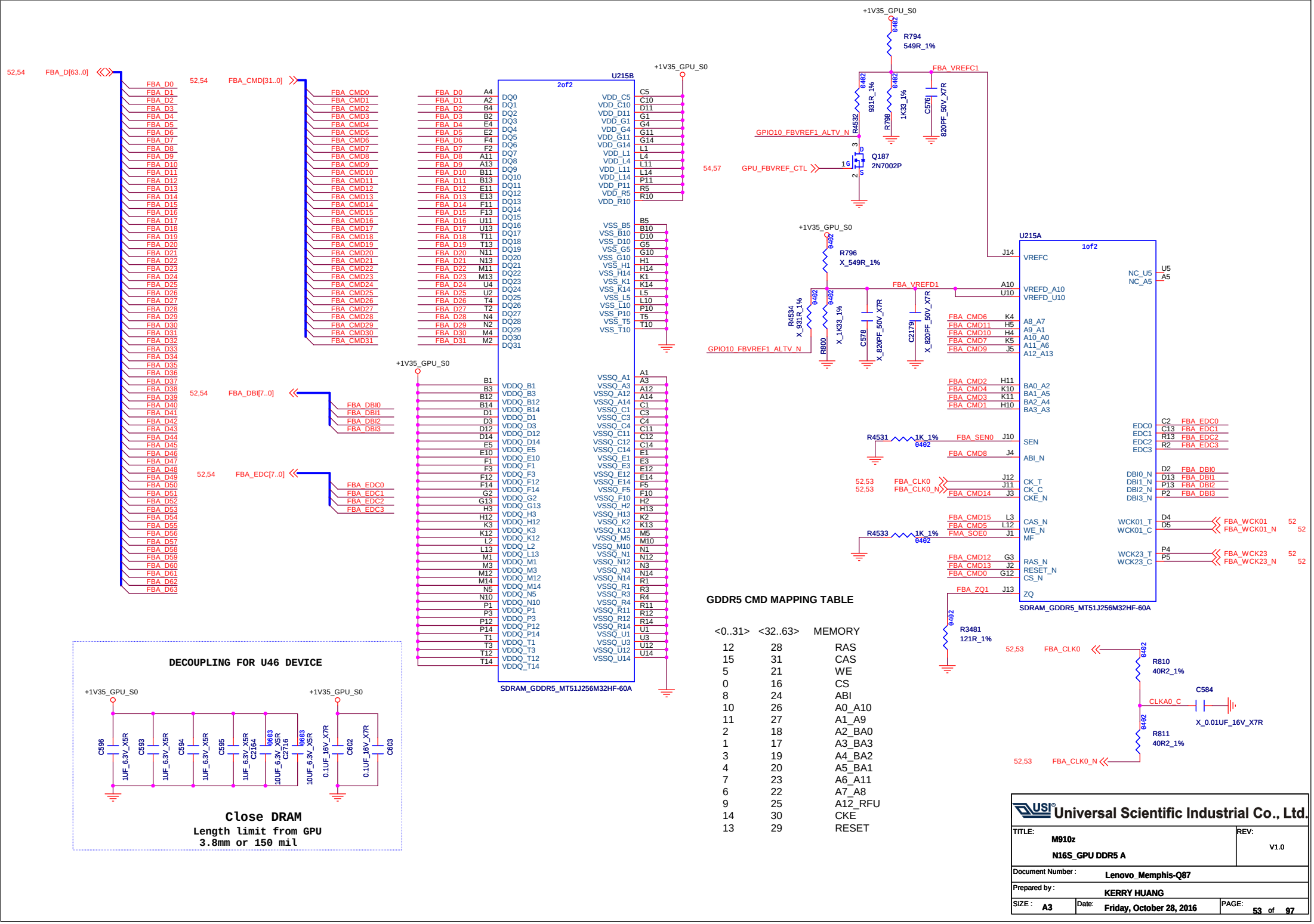
| | |
|---|---|
| TITLE: M910z N16S_MEMORY | REV: V1.0 |
| Document Number : | |
| Prepared by : KERRY HUANG | |
| SIZE : Custom | Date: Friday, October 28, 2016 |
| PAGE: 52 of 97 | |

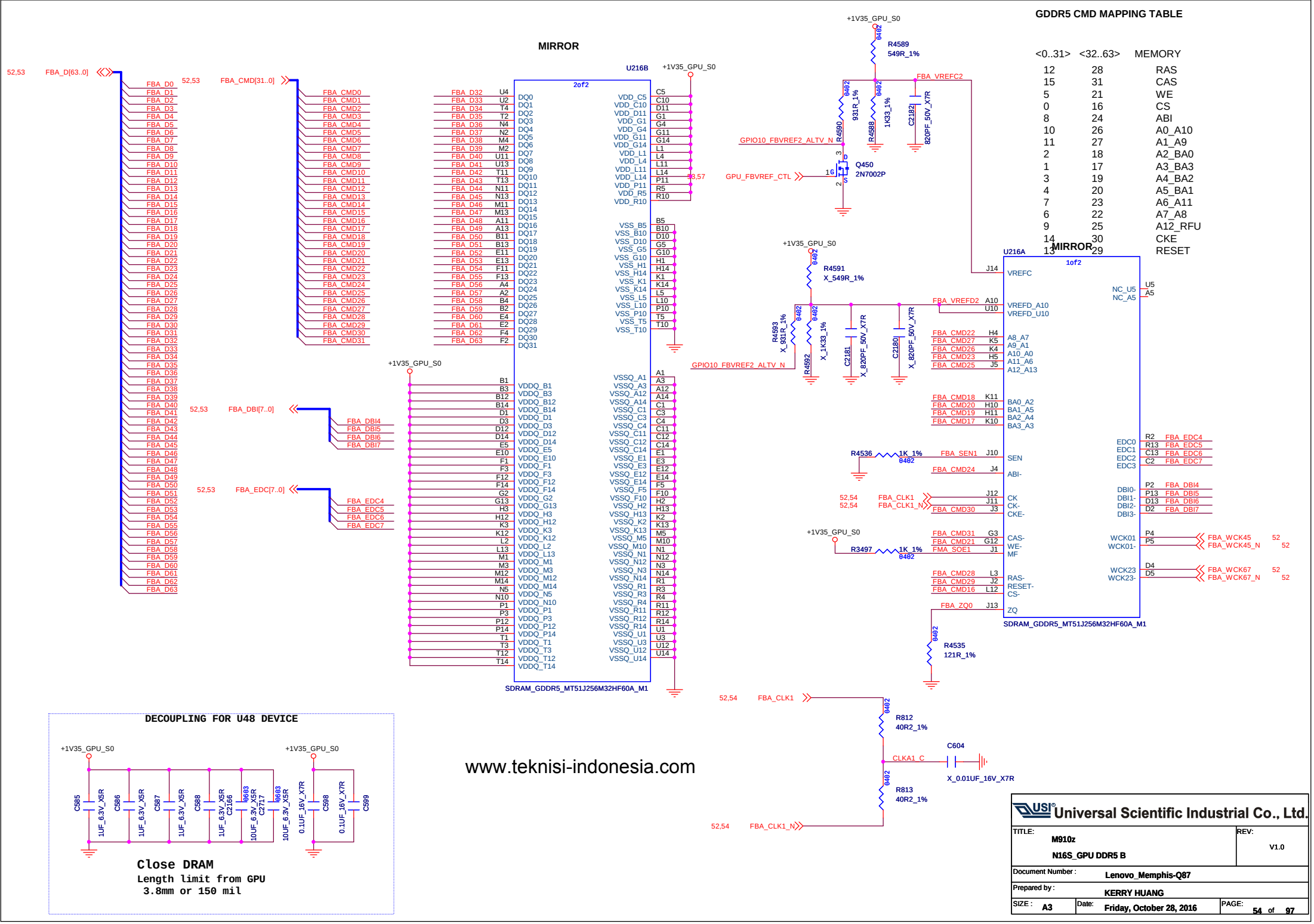


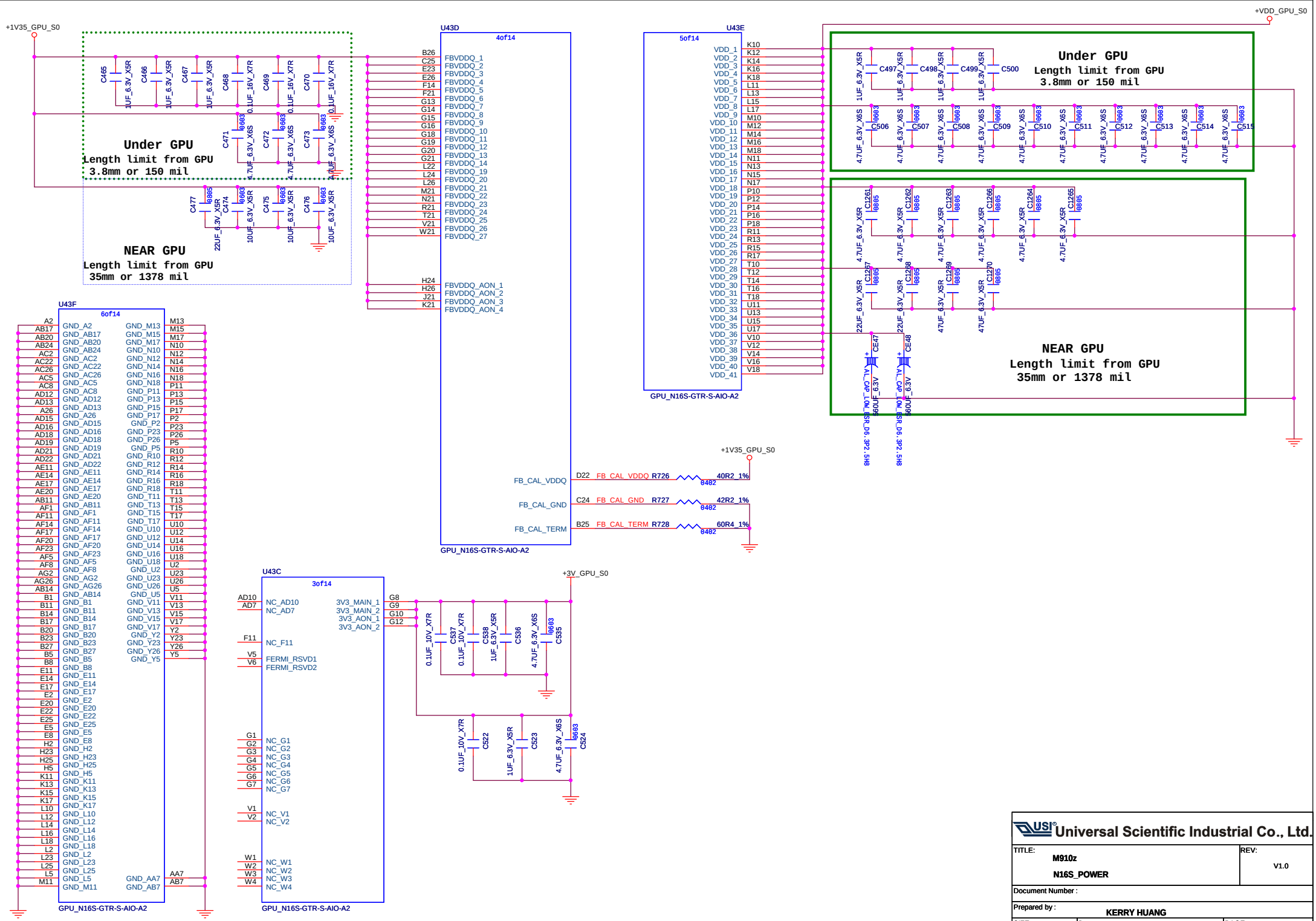

**GDDR5 CMD MAPPING TABLE**

| <0..31> | <32..63> | MEMORY |
|---|---|---|
| 12 | 28 | RAS |
| 15 | 31 | CAS |
| 5 | 21 | WE |
| 0 | 16 | CS |
| 8 | 24 | ABI |
| 10 | 26 | A0_A10 |
| 11 | 27 | A1_A9 |
| 2 | 18 | A2_BA0 |
| 1 | 17 | A3_BA3 |
| 3 | 19 | A4_BA2 |
| 4 | 20 | A5_BA1 |
| 7 | 23 | A6_A11 |
| 6 | 22 | A7_A8 |
| 9 | 25 | A12_RFU |
| 14 | 30 | CKE |
| 13 | 29 | RESET |

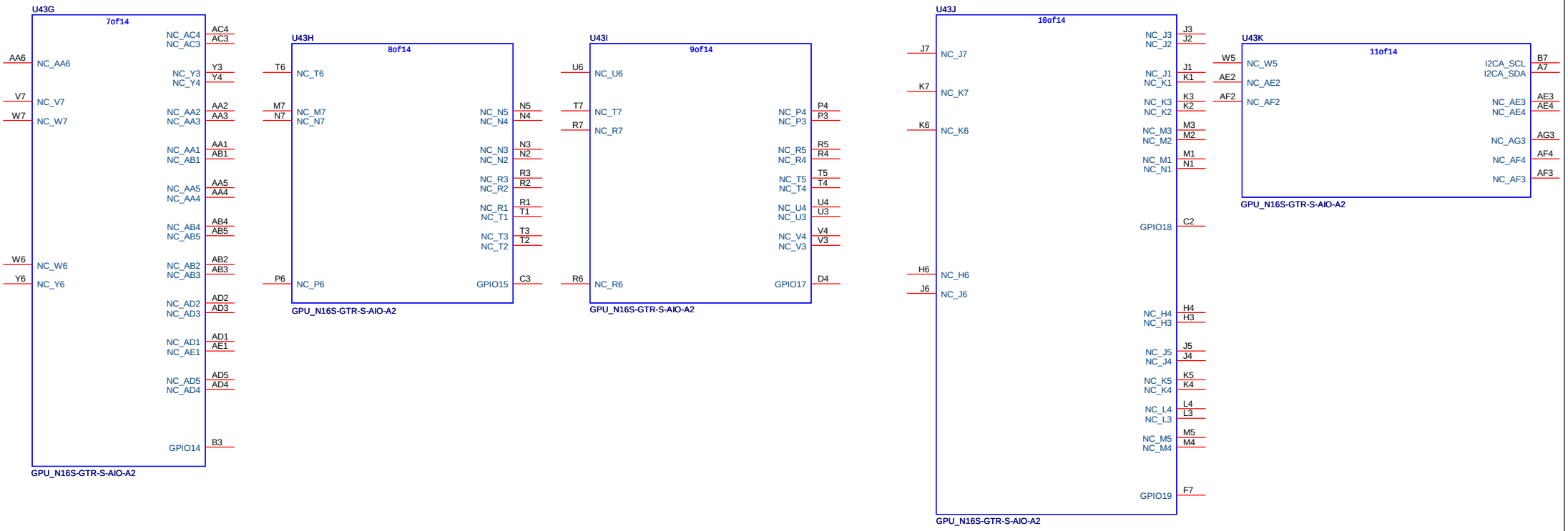
Universal Scientific Industrial Co., Ltd.

| | | |
|---|---|---|
| TITLE: M910z N16S_GPU DDR5 A | | REV: V1.0 |
| Document Number : Lenovo_Memphis-Q87 | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 53 of 97 |


GDDR5 CMD MAPPING TABLE
<0..31> <32..63> MEMORY
12 28 RAS
15 31 CAS
5 21 WE
0 16 CS
8 24 ABI
10 26 A0_A10
11 27 A1_A9
2 18 A2_BA0
1 17 A3_BA3
3 19 A4_BA2
4 20 A5_BA1
7 23 A6_A11
6 22 A7_A8
9 25 A12_RFU
14 30 CKE
13 29 RESET
MIRROR
MIRROR
FBA_D[63..0]
FBA_CMD[31..0]
FBA_DBI[7..0]
FBA_EDC[7..0]
U216B
U216A
2of2
1of2
SDRAM_GDDR5_MT51J256M32HF60A_M1
SDRAM_GDDR5_MT51J256M32HF60A_M1
+1V35_GPU_S0
R4589 549R_1%
R4590 931R_1%
R4588 1K33_1%
C2182 820PF_50V_X7R
FBA_VREFC2
GPIO10_FBVREF2_ALTV_N
GPU_FBVREF_CTL
Q450 2N7002P
R4591 X_549R_1%
R4593 X_931R_1%
R4592 X_1K33_1%
C2181 X_820PF_50V_X7R
C2180 X_820PF_50V_X7R
R4536 1K_1%
R3497 1K_1%
R4535 121R_1%
R812 40R2_1%
R813 40R2_1%
C604 X_0.01UF_16V_X7R
FBA_CLK1
FBA_CLK1_N
FBA_SEN1
FBA_ZQ0
FBA_WCK45
FBA_WCK45_N
FBA_WCK67
FBA_WCK67_N
DECOUPLING FOR U48 DEVICE
C585 1UF_6.3V_X5R
C586 1UF_6.3V_X5R
C587 1UF_6.3V_X5R
C588 1UF_6.3V_X5R
C2166 10603
C2717 10UF_6.3V_X5R
10UF_6.3V_X5R
C598 0.1UF_16V_X7R
C599 0.1UF_16V_X7R
Close DRAM
Length limit from GPU
3.8mm or 150 mil
www.teknisi-indonesia.com
Universal Scientific Industrial Co., Ltd.
TITLE: M910z
N16S_GPU DDR5 B
REV: V1.0
Document Number : Lenovo_Memphis-Q87
Prepared by : KERRY HUANG
SIZE : A3
Date: Friday, October 28, 2016
PAGE: 54 of 97




| | |
|---|---|
| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M910z N16S_POWER | REV: V1.0 |
| Document Number : | |
| Prepared by : KERRY HUANG | |
| SIZE : A3 | Date: Friday, October 28, 2016 |
| PAGE: 55 of 97 | |

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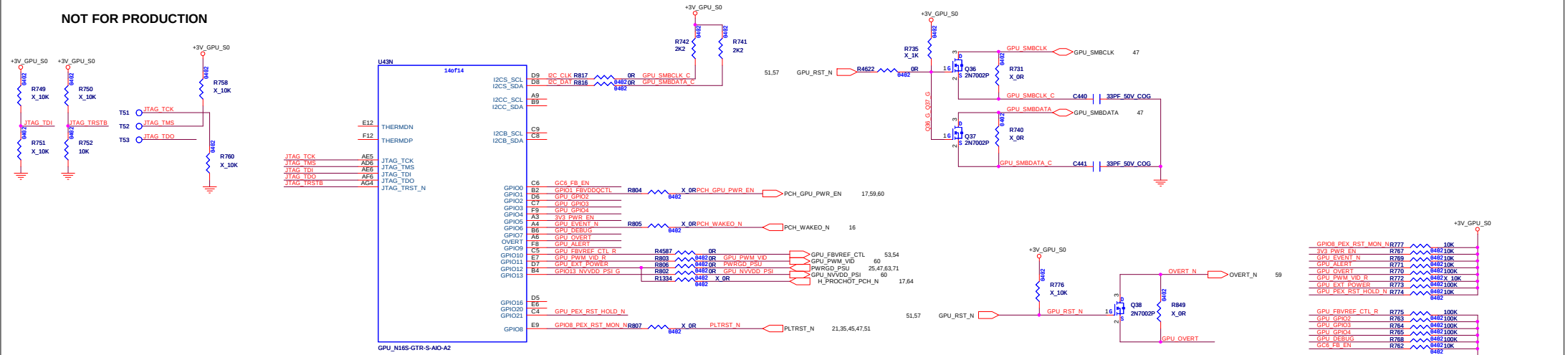
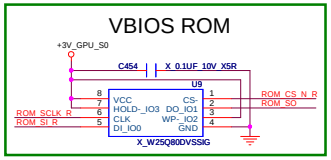
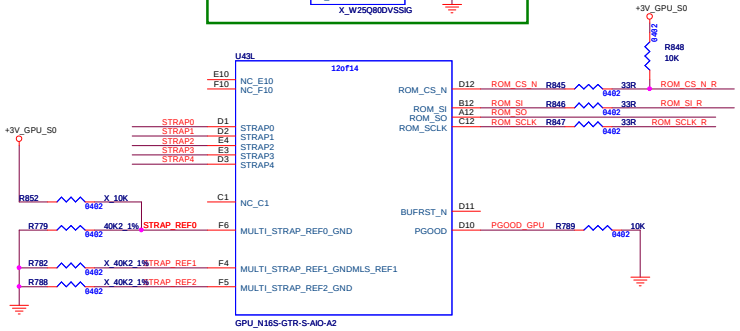
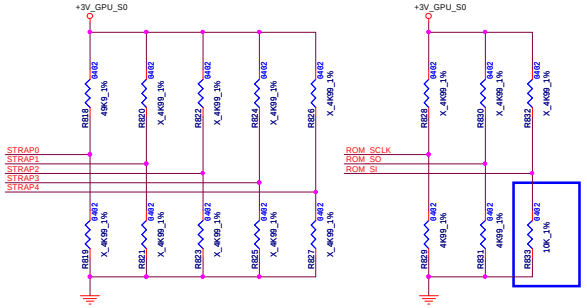
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z N16S_IFP/DAC | | REV: V1.0 |
| Document Number : | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 56 of 97 |

NOT FOR PRODUCTION







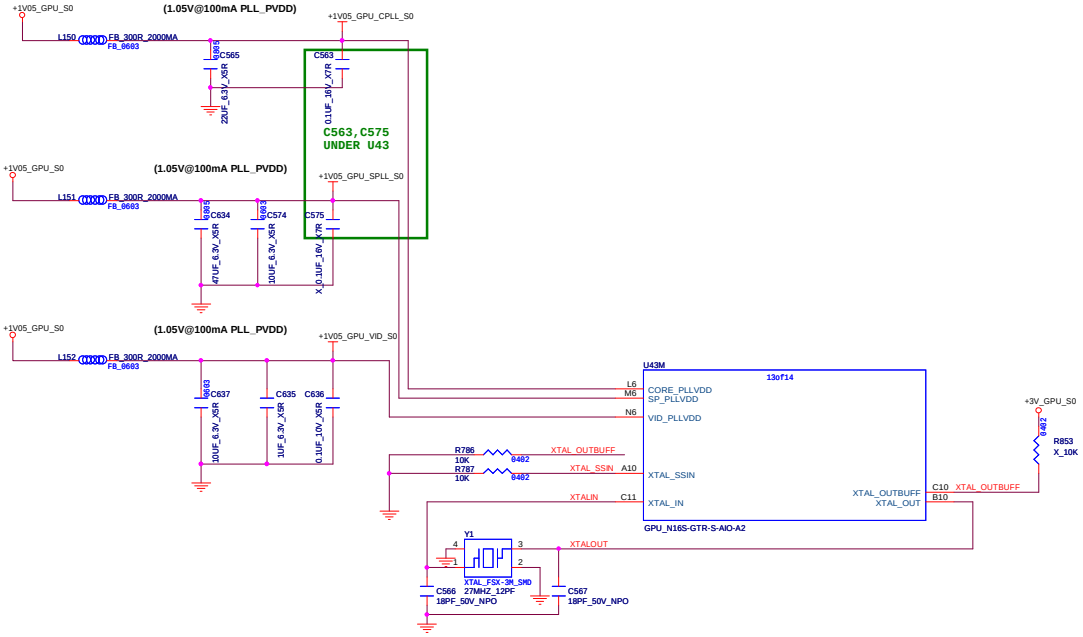
| MEMORY CONFIG | SI | DESCRIPTION |
|---|---|---|
| MICRON 8Gb | 0001 (10K to GND) | MT51J256M32HF-60:A (Default) |
| SAMSUNG 8Gb | 0000(4K99 to GND) | K4G80325FB-HC03 |

| Resistor Values | Pull-Up to 3V3_MAIN | Pull-Down to GND |
|---|---|---|
| 4.99 kΩ | 1000 | 0000 |
| 10.0 kΩ | 1001 | 0001 |
| 15.0 kΩ | 1010 | 0010 |
| 20.0 kΩ | 1011 | 0011 |
| 24.9 kΩ | 1100 | 0100 |
| 30.1 kΩ | 1101 | 0101 |
| 34.8 kΩ | 1110 | 0110 |
| 45.3 kΩ | 1111 | 0111 |

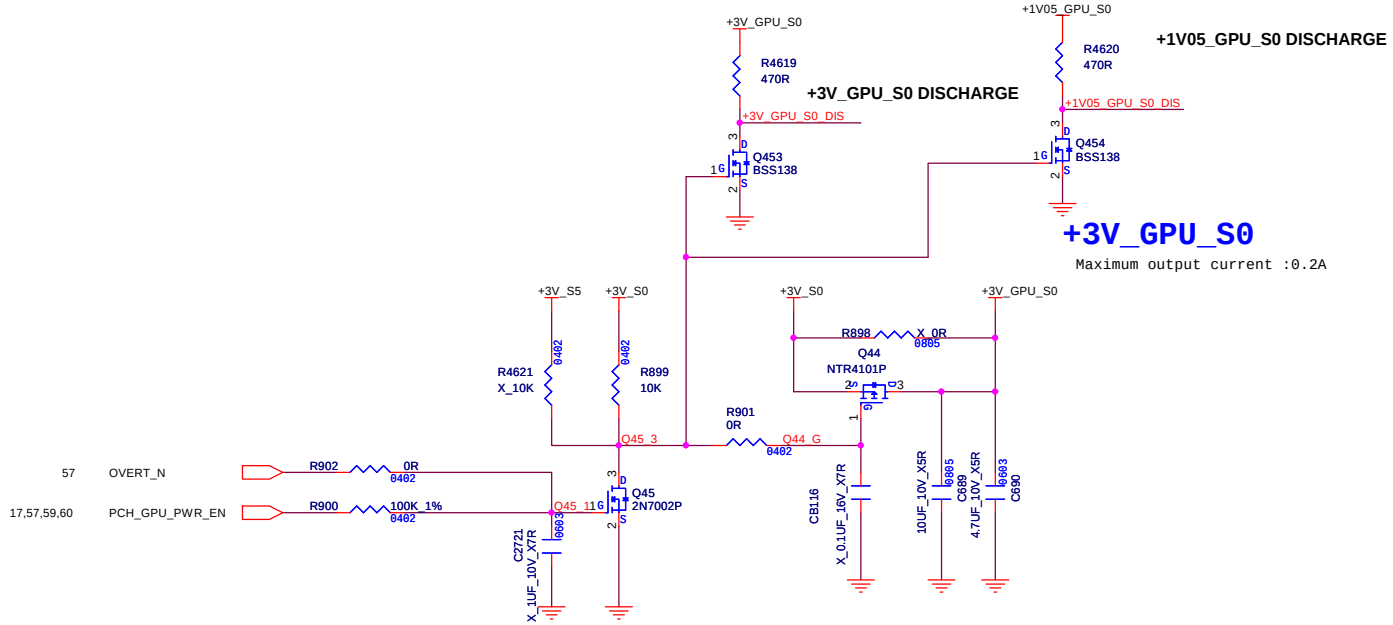
COMPRESSED IMAGE

Universal Scientific Industrial Co., Ltd.

| | | | |
|---|---|---|---|
| TITLE: M910z N16S_IO | | | REV: V1.0 |
| Document Number : | | | |
| Prepared by : | KERRY HUANG | | |
| SIZE : A2 | Date: Friday, October 28, 2016 | | PAGE: 57 of 97 |




| | | |
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z N16S_XTAL | | REV: V1.0 |
| Document Number : | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A2 | Date: Friday, October 28, 2016 | PAGE: 58 of 97 |

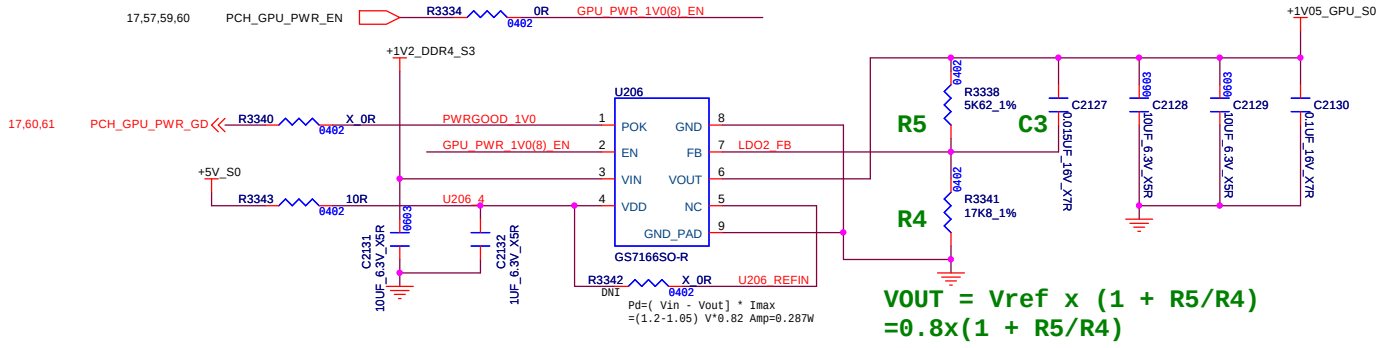



| Parameter | Value |
|---|---|
| Output voltage | 1.05V |
| Maximum output current | 2.1A |
| IC current limit | TBD |
| Max. PD(theoretically) | 0.123W |
| Rja | 50 °C/W |
| Enable condition | "PCH_GPU_PWR_EN" is High |

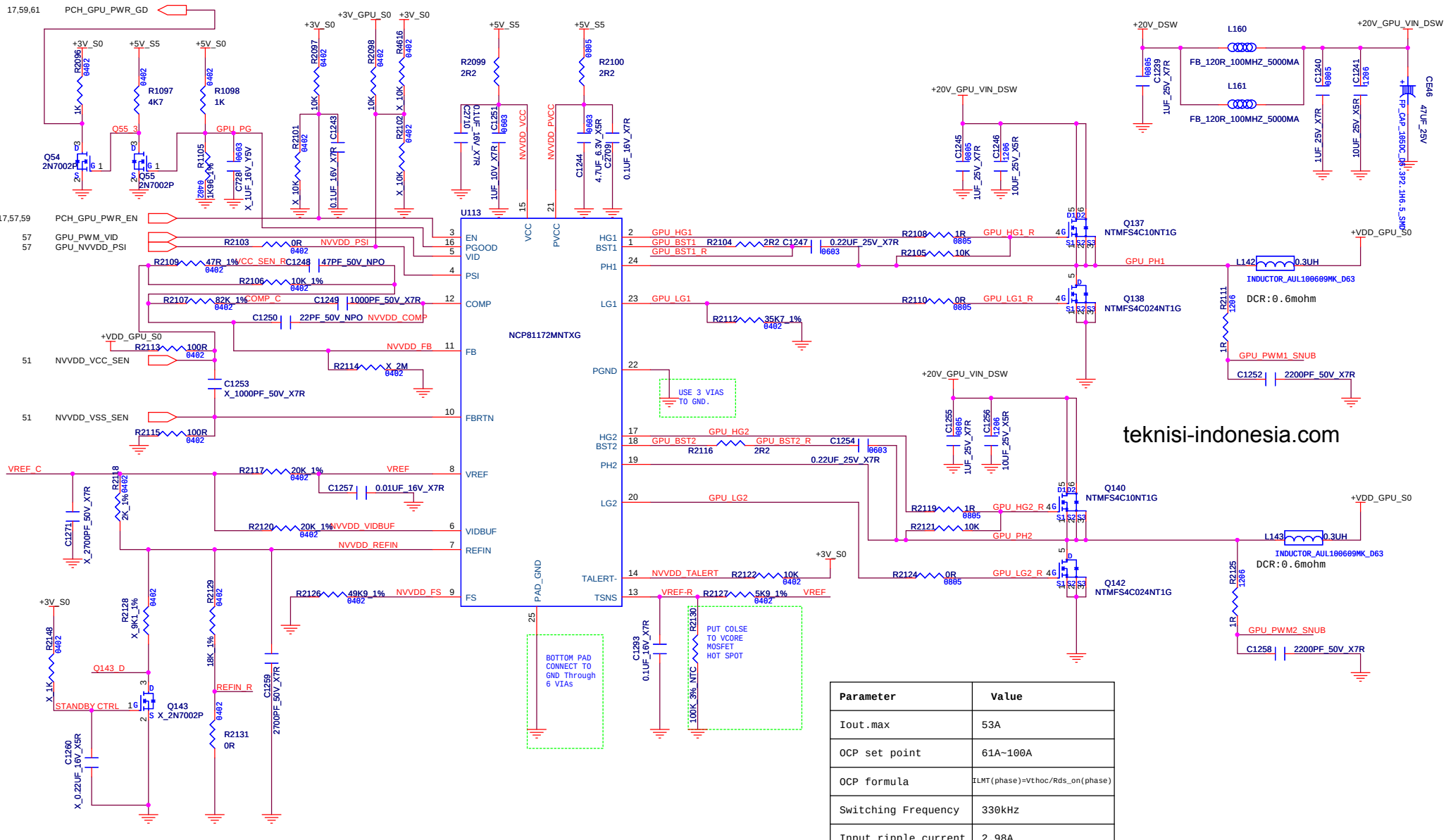
SLP_S3:
LOW:Disable SM
HIGH: Enable SM

**LDO: Vin = +1.2V Vout = +1.05V +/- 30mV Iout = 0.82A MAX**

**PCB: 50 to 70mm sq. copper area for cooling**




| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z<br>+3V_GPU_S0_+1V05_GPU_S0 | | | REV: V1.0 |
| Document Number : | Lenovo_Memphis-Q87 | | |
| Prepared by : | KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 59 of 97 | |

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| Parameter | Value |
|---|---|
| Iout.max | 53A |
| OCP set point | 61A~100A |
| OCP formula | ILMT(phase)=Vthoc/Rds_on(phase) |
| Switching Frequency | 330kHz |
| Input ripple current | 2.98A |
| Output ripple current | 2.48A |
| Choke_size(L*W*H)(mm) | 10.8*7.0*10.0 |
| Choke_Isat | 40A |
| Choke_DCR | 0.60mΩ |
| Choke_LIR | 62.5% |
| Input capacitance | 10UF_25V_X5R_0805*1<br>1UF_25V_X7R_0805*2 |
| Output capacitance (Near GPU side) | 560UF_6.3V*2<br>47UF_6.3V_X5R_0805*4<br>4.7UF_6.3V_X5R_0805*10 |

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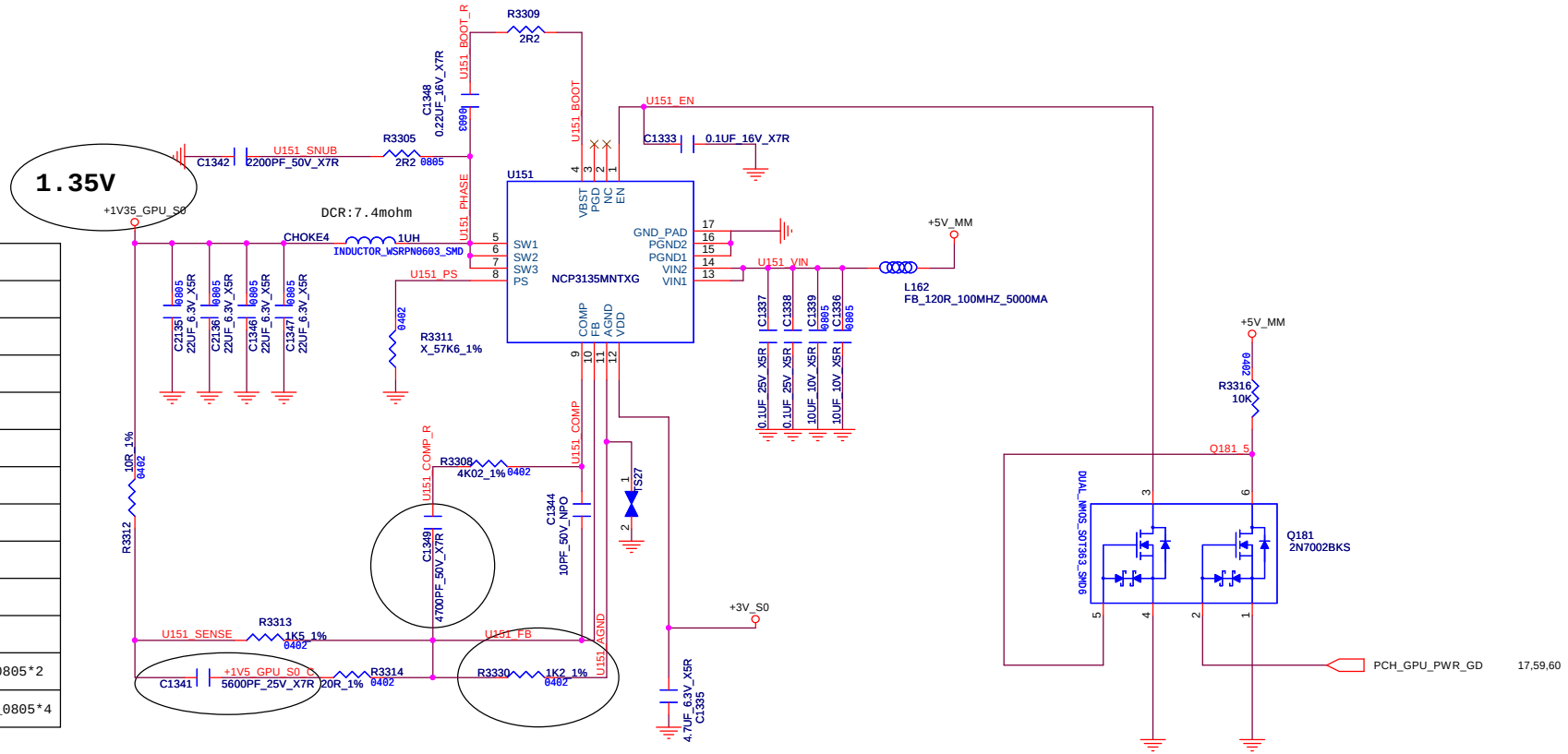
| | | |
|---|---|---|
| TITLE: M910z N16S NVVDD | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 60 of 97 |

# GDDR5 1.35V POWER

## 1.35V

| Parameter | Value |
|---|---|
| Iout.max | 4.1A |
| OCP set point | TBD |
| OCP formula | IC controlled |
| Switching Frequency | 330kHz |
| Input ripple current | 1.33A |
| Output ripple current | 1.05A |
| Choke_size(L*W*H)(mm) | 7.6*6.8*3.0 |
| Choke_Isat | 15A |
| Choke_DCR | 7.40mΩ |
| Choke_LIR | 27.5% |
| Input capacitance | 10UF_10V_X5R_0805*2 |
| Output capacitance | 22UF_6.3V_X5R_0805*4 |

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|---|---|
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| TITLE: M910z N16S FBVDD | REV: V1.0 |
| Document Number : <Doc> | |
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| SIZE : A3 | Date: Tuesday, November 01, 2016 |
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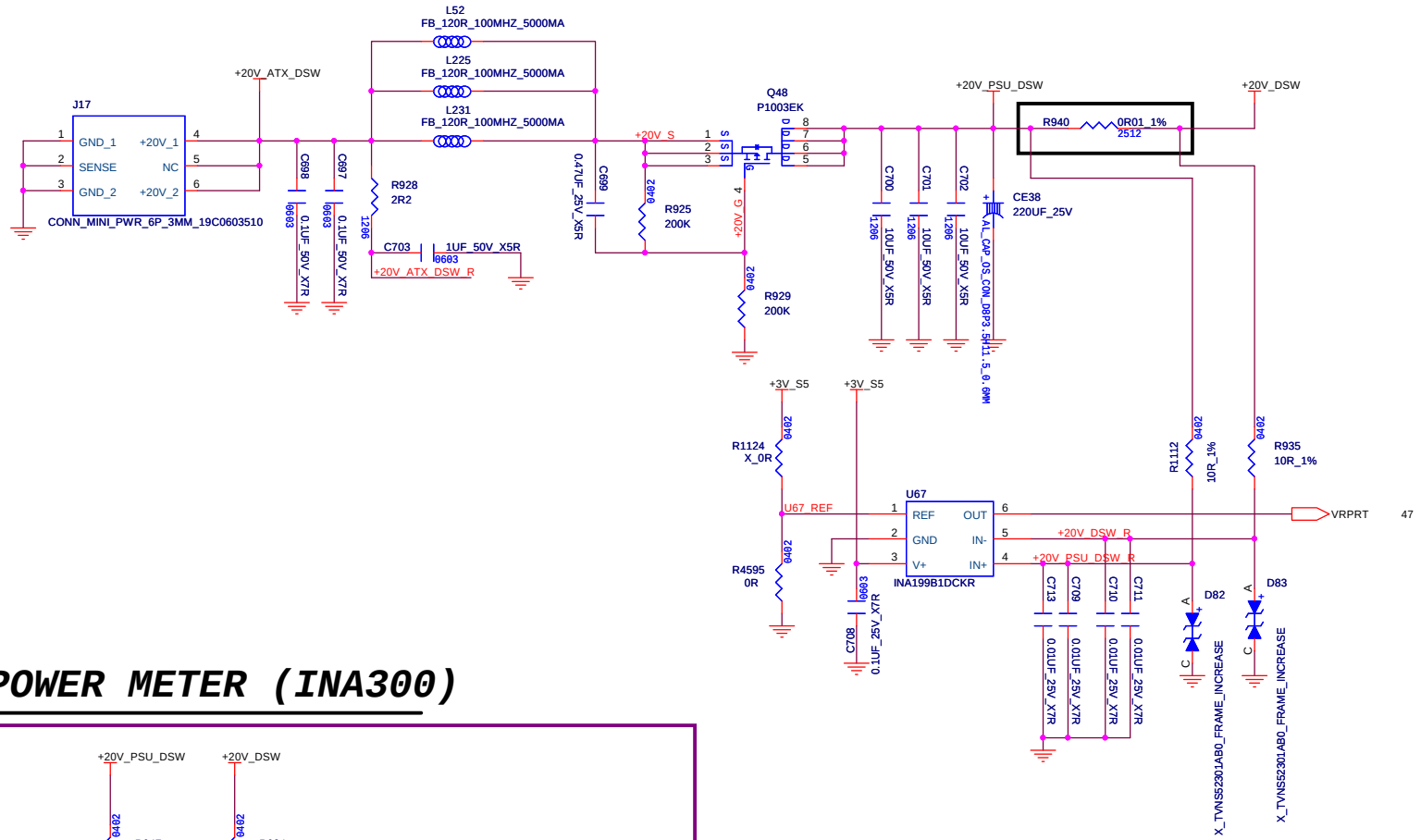
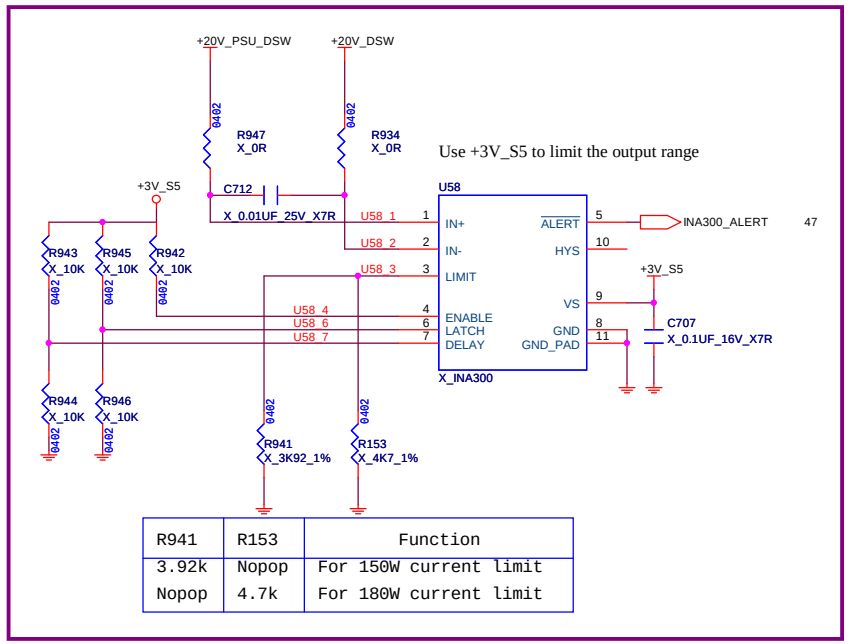
# ATX 20V POWER




# POWER METER (INA300)




| R941 | R153 | Function |
|---|---|---|
| 3.92k | Nopop | For 150W current limit |
| Nopop | 4.7k | For 180W current limit |

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| | | |
|---|---|---|
| TITLE: M910z DC IN | | REV: V1.0 |
| Document Number : <Doc> | | |
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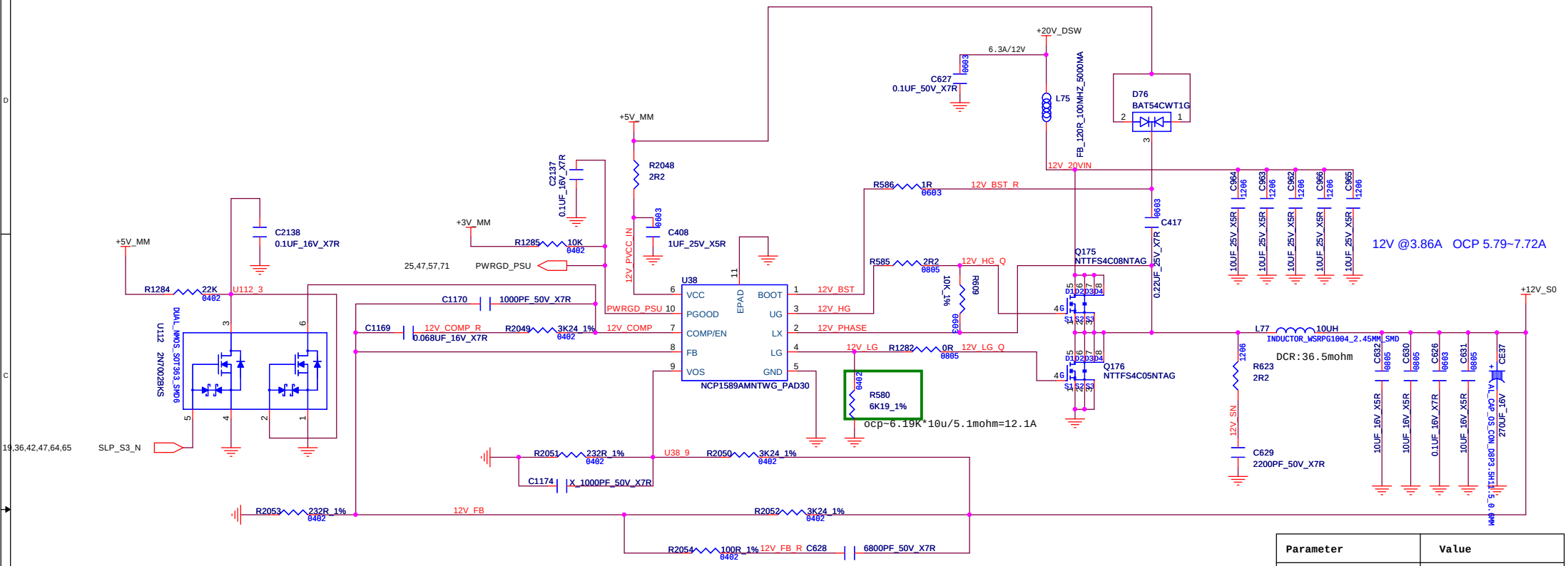
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 62 of 97 |




| Parameter | Value |
|---|---|
| Iout.max | 3.86A |
| OCP set point | 12.1A |
| OCP formula | ROCSET*10uA/Rds_on |
| Switching Frequency | 300kHz |
| Input ripple current | 1.41A |
| Output ripple current | 0.47A |
| Choke_size(L*W*H)(mm) | 7.6*6.8*3 |
| Choke_Isat | 5.5A |
| Choke_DCR | 68.00mΩ |
| Choke_LIR | 41.5% |
| Input capacitance | 10UF_25V_X5R_1206*5 |
| Output capacitance | 270UF_16V*1<br>10UF_16V_X5R_0805*3 |

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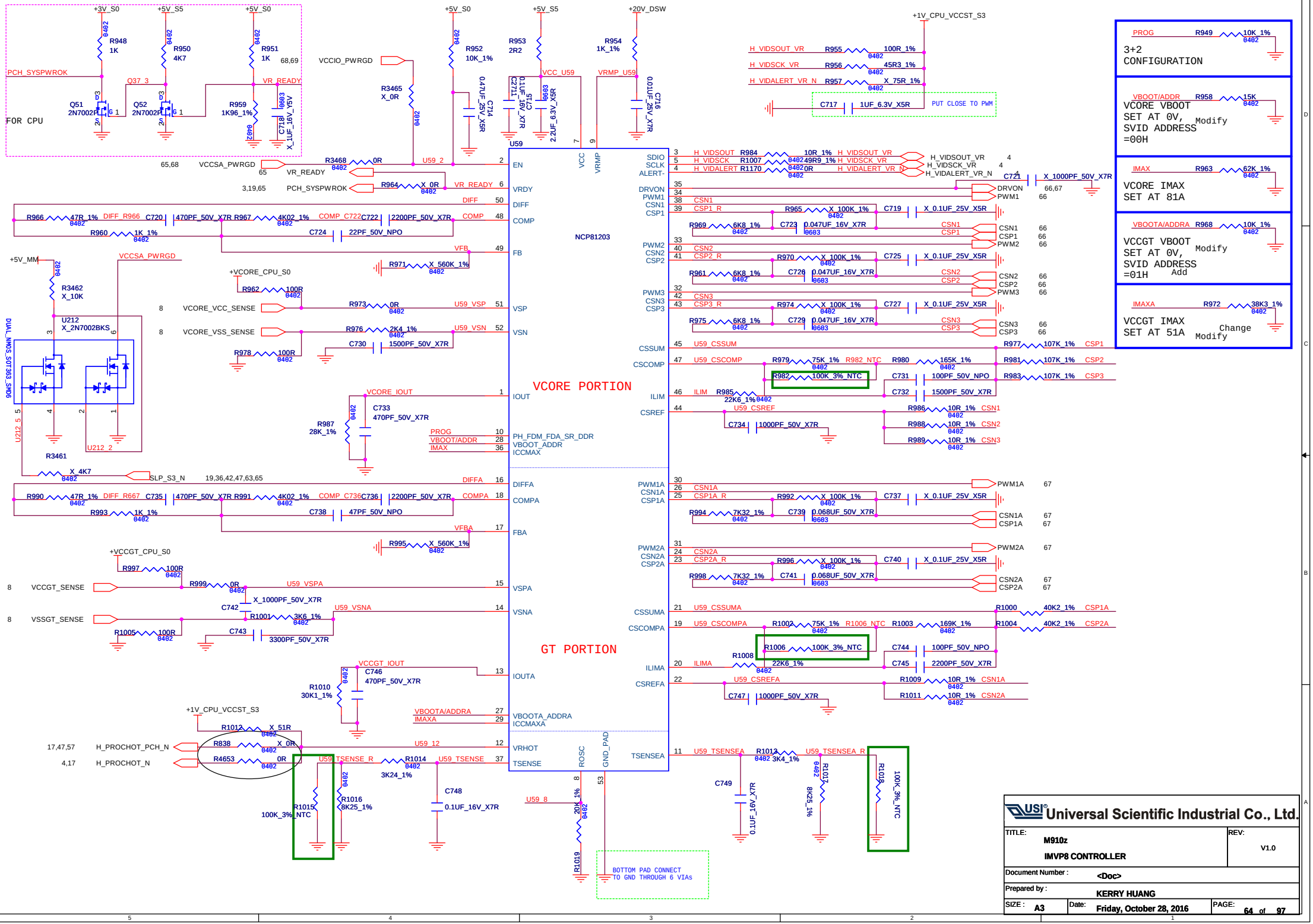
| | | |
|---|---|---|
| TITLE: M910z<br>20V TO 12V | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 63 of 97 |


NCP81203
VCORE PORTION
GT PORTION
FOR CPU
PCH_SYSPWROK
VR_READY
VCCIO_PWRGD
VCCSA_PWRGD
PCH_SYSPWROK
VCC_U59
VRMP_U59
+1V_CPU_VCCST_S3
H_VIDSOUT_VR
H_VIDSCK_VR
H_VIDALERT_VR_N
PUT CLOSE TO PWM
PROG
3+2
CONFIGURATION
VBOOT/ADDR
VCORE VBOOT
SET AT 0V,
SVID ADDRESS
=00H
Modify
IMAX
VCORE IMAX
SET AT 81A
VBOOTA/ADDRA
VCCGT VBOOT
SET AT 0V,
SVID ADDRESS
=01H
Add
IMAXA
VCCGT IMAX
SET AT 51A
Change
Modify
+5V_MM
+VCORE_CPU_S0
+VCCGT_CPU_S0
VCORE_VCC_SENSE
VCORE_VSS_SENSE
VCCGT_SENSE
VSSGT_SENSE
SLP_S3_N
H_PROCHOT_PCH_N
H_PROCHOT_N
BOTTOM PAD CONNECT
TO GND THROUGH 6 VIAs
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TITLE:
M910z
IMVP8 CONTROLLER
REV:
V1.0
Document Number :
<Doc>
Prepared by :
KERRY HUANG
SIZE :
A3
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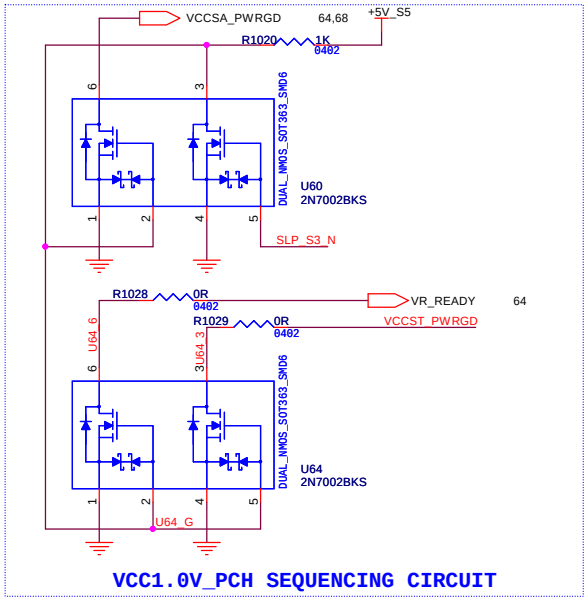
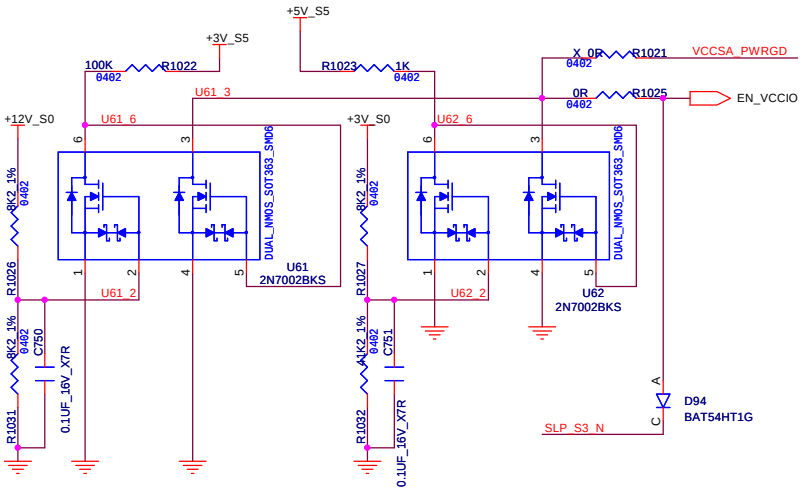
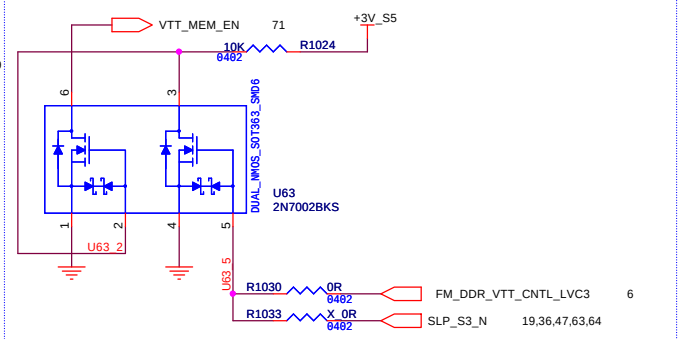


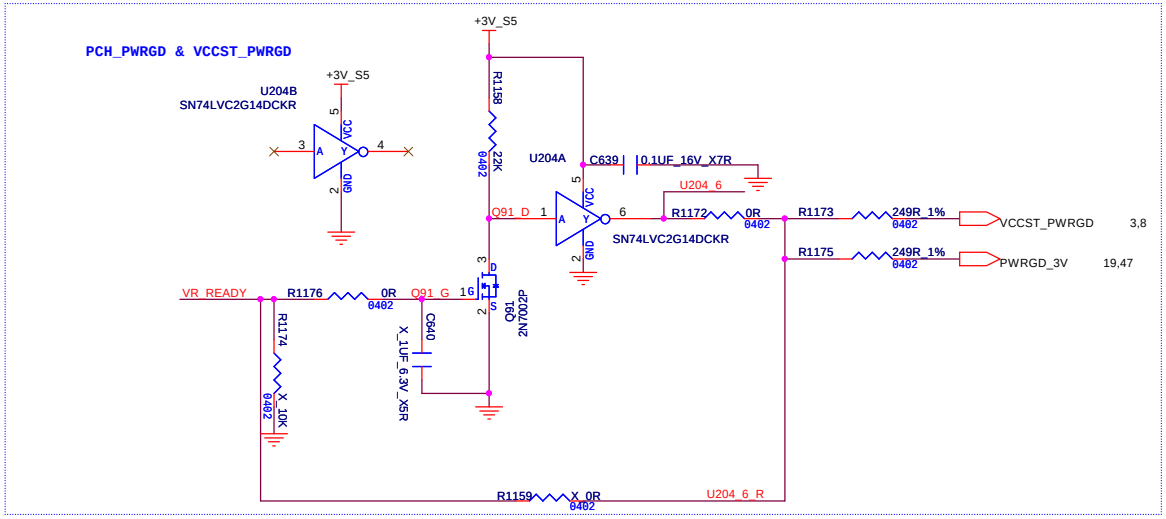

VCC1.0V_PCH SEQUENCING CIRCUIT

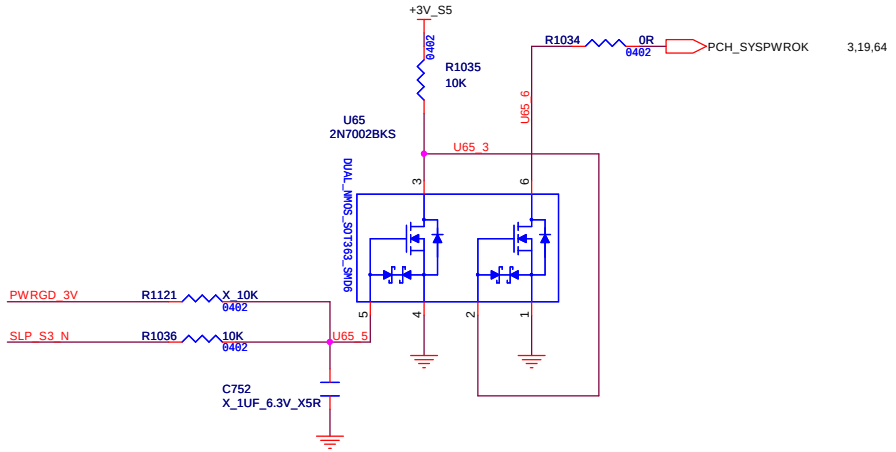



VR_ENABLE, VCCSA_EN




VTT_MEM_EN CIRCUIT




| | | |
|---|---|---|
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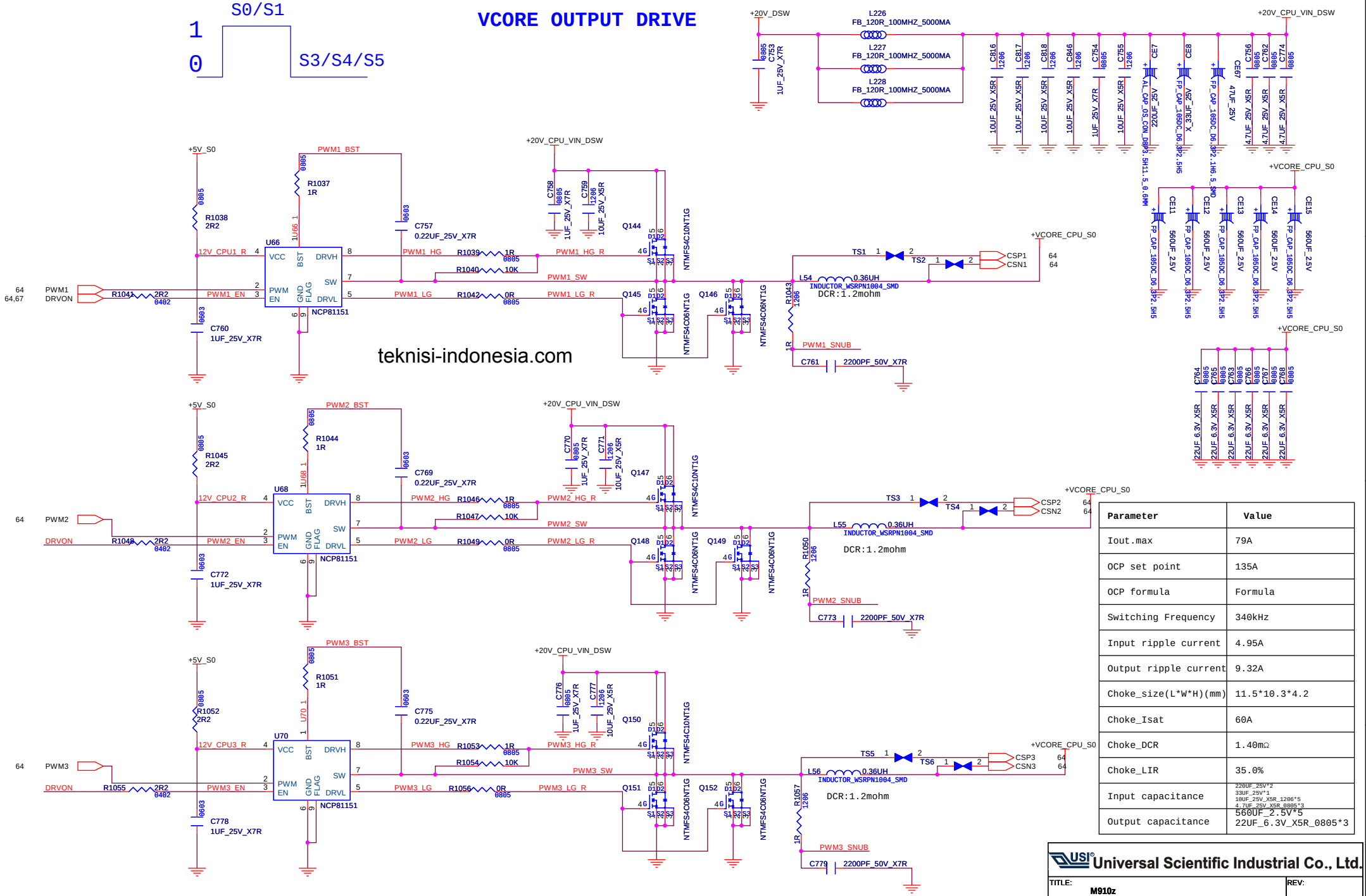
| TITLE: M910z<br>IMVP8 _VR_EN CONTROL | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 65 of 97 |

# VCORE OUTPUT DRIVE




| Parameter | Value |
|---|---|
| Iout.max | 79A |
| OCP set point | 135A |
| OCP formula | Formula |
| Switching Frequency | 340kHz |
| Input ripple current | 4.95A |
| Output ripple current | 9.32A |
| Choke_size(L*W*H)(mm) | 11.5*10.3*4.2 |
| Choke_Isat | 60A |
| Choke_DCR | 1.40mΩ |
| Choke_LIR | 35.0% |
| Input capacitance | 220UF_25V*2<br>33UF_25V*1<br>10UF_25V_X5R_1206*5<br>4.7UF_25V_X5R_0805*3 |
| Output capacitance | 560UF_2.5V*5<br>22UF_6.3V_X5R_0805*3 |

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| | | |
|---|---|---|
| TITLE: M910z VCORE OUTPUT DRIVEVE | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
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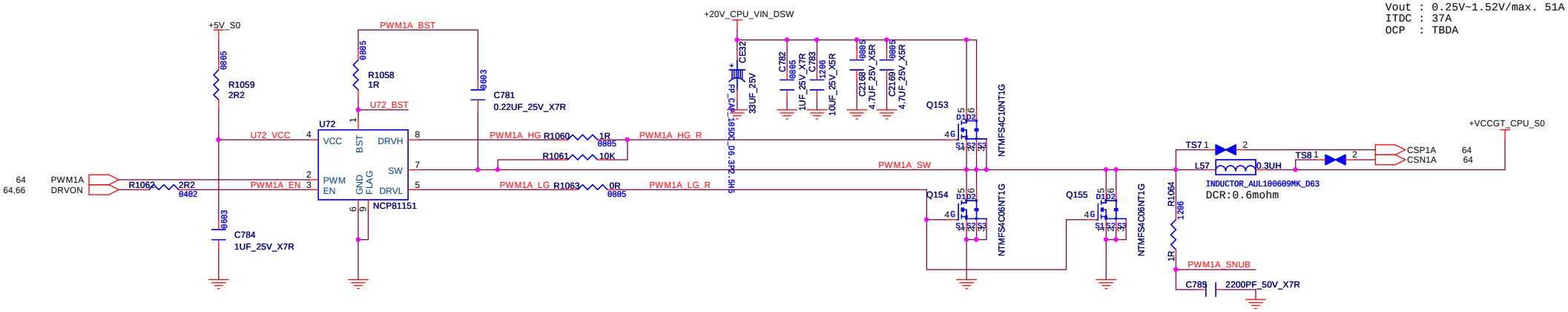
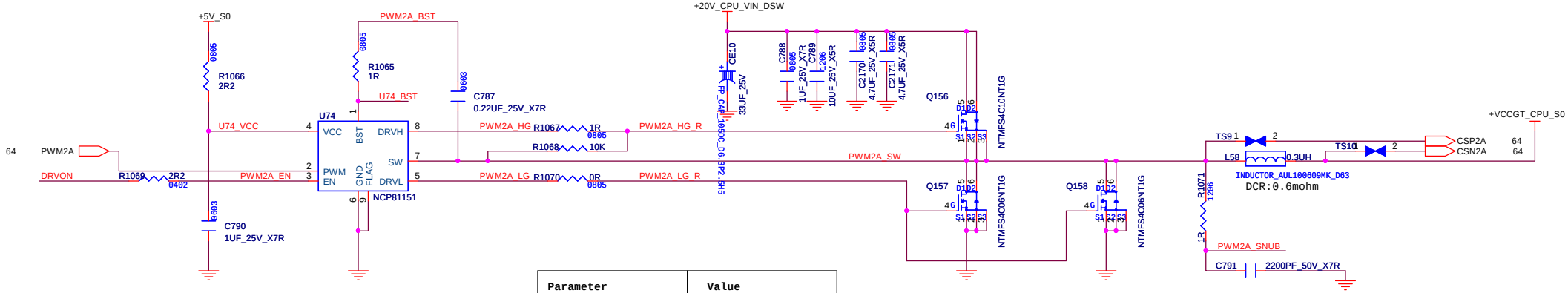
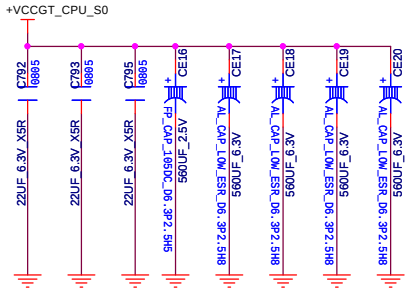
# +VCCGT_CPU_S0

Vin : 20V
Vout : 0.25V~1.52V/max. 51A
ITDC : 37A
OCP : TBDA




| Parameter | Value |
|---|---|
| Iout.max | 51A |
| OCP set point | 90A |
| OCP formula | Formula |
| Switching Frequency | 340kHz |
| Input ripple current | 5.47 |
| Output ripple current | 10.95 |
| Choke_size(L*W*H)(mm) | 10.8*7.0*10.0 |
| Choke_Isat | 40 |
| Choke_DCR | 0.60mΩ |
| Choke_LIR | 43.3% |
| Input capacitance | 220UF_25V*1<br>10UF_25V_X5R_1206*1 |
| Output capacitance | 560UF_6.3V*4<br>560UF_2.5V*1<br>22UF_6.3V_X5R_0805*3 |

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| | | |
|---|---|---|
| TITLE: M910z<br>VCCGT OUTPUT DRIVE | | REV: V1.0 |
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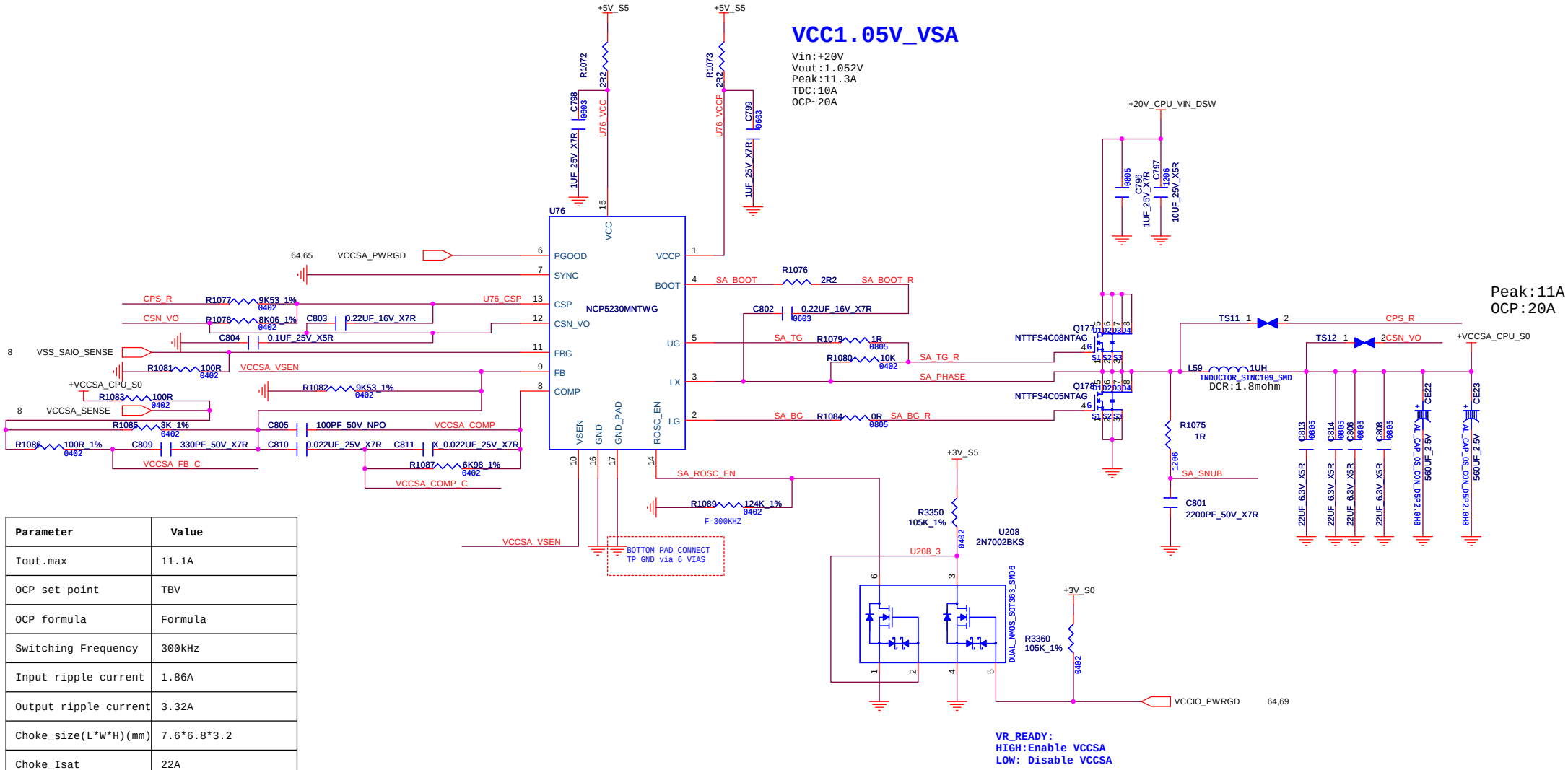
# VCC1.05V_VSA

Vin:+20V
Vout:1.052V
Peak:11.3A
TDC:10A
OCP~20A




Peak:11A
OCP:20A

| Parameter | Value |
|---|---|
| Iout.max | 11.1A |
| OCP set point | TBV |
| OCP formula | Formula |
| Switching Frequency | 300kHz |
| Input ripple current | 1.86A |
| Output ripple current | 3.32A |
| Choke_size(L*W*H)(mm) | 7.6*6.8*3.2 |
| Choke_Isat | 22A |
| Choke_DCR | 10.00mΩ |
| Choke_LIR | 29.9% |
| Input capacitance | 10UF_25V_X5R_1206*1 |
| Output capacitance | 560UF_2.5V*1<br>22UF_6.3V_X5R_0805*4 |

**VR_READY:**
**HIGH:Enable VCCSA**
**LOW: Disable VCCSA**

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| | | |
|---|---|---|
| TITLE: M910z VCCSA OUTPUT DRIVE | | REV: V1.0 |
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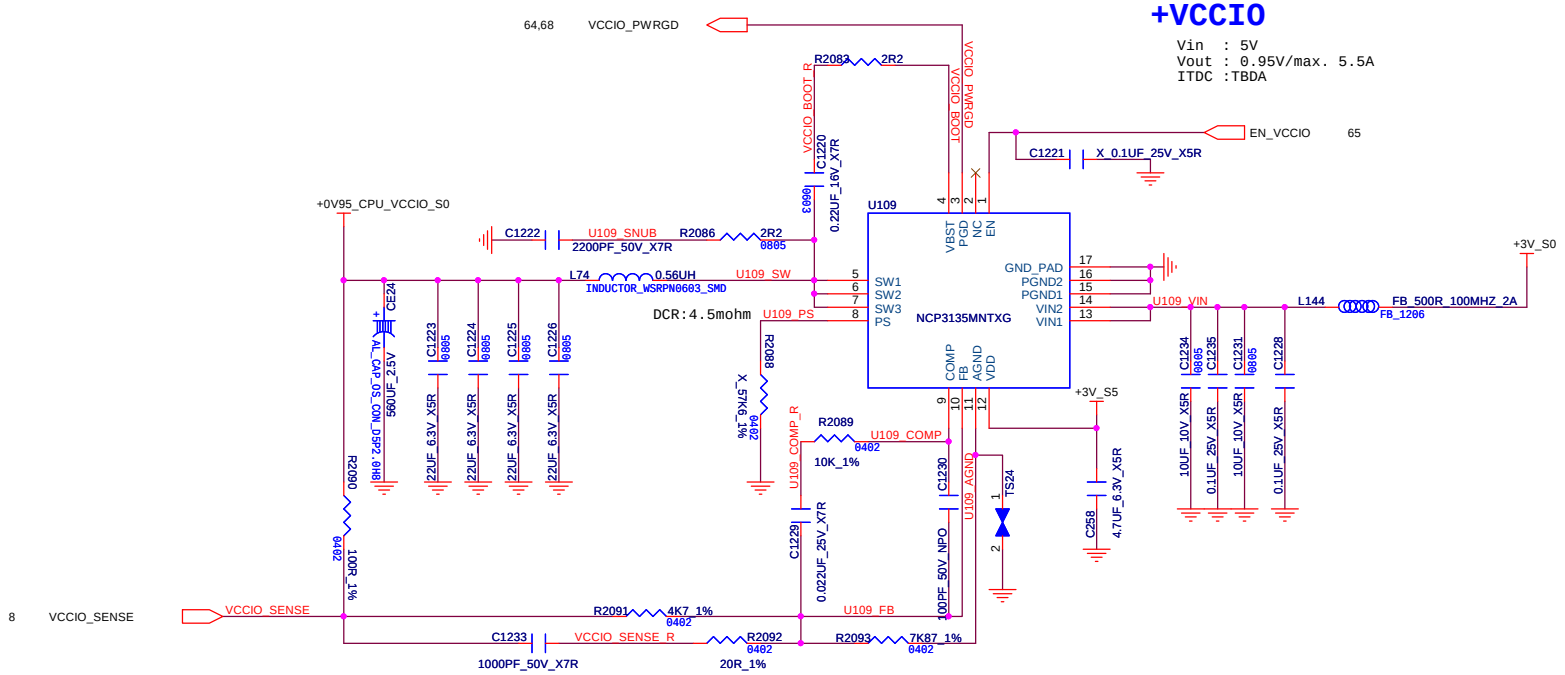


| Parameter | Value |
|---|---|
| Iout.max | 5.5A |
| OCP set point | 6.8A |
| OCP formula | IC controlled |
| Switching Frequency | 1MHz |
| Input ripple current | 1.62A |
| Output ripple current | 1.64A |
| Choke_size(L*W*H)(mm) | 7.6*6.8*3 |
| Choke_Isat | 18A |
| Choke_DCR | 4.50mΩ |
| Choke_LIR | 29.7% |
| Input capacitance | 10UF_10V_X5R_0805*2 |
| Output capacitance | 560UF_2.5V*1<br>22UF_6.3V_X5R_0805*4 |

| | | | |
|---|---|---|---|
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| TITLE: M910z VCCIO | | | REV: V1.0 |
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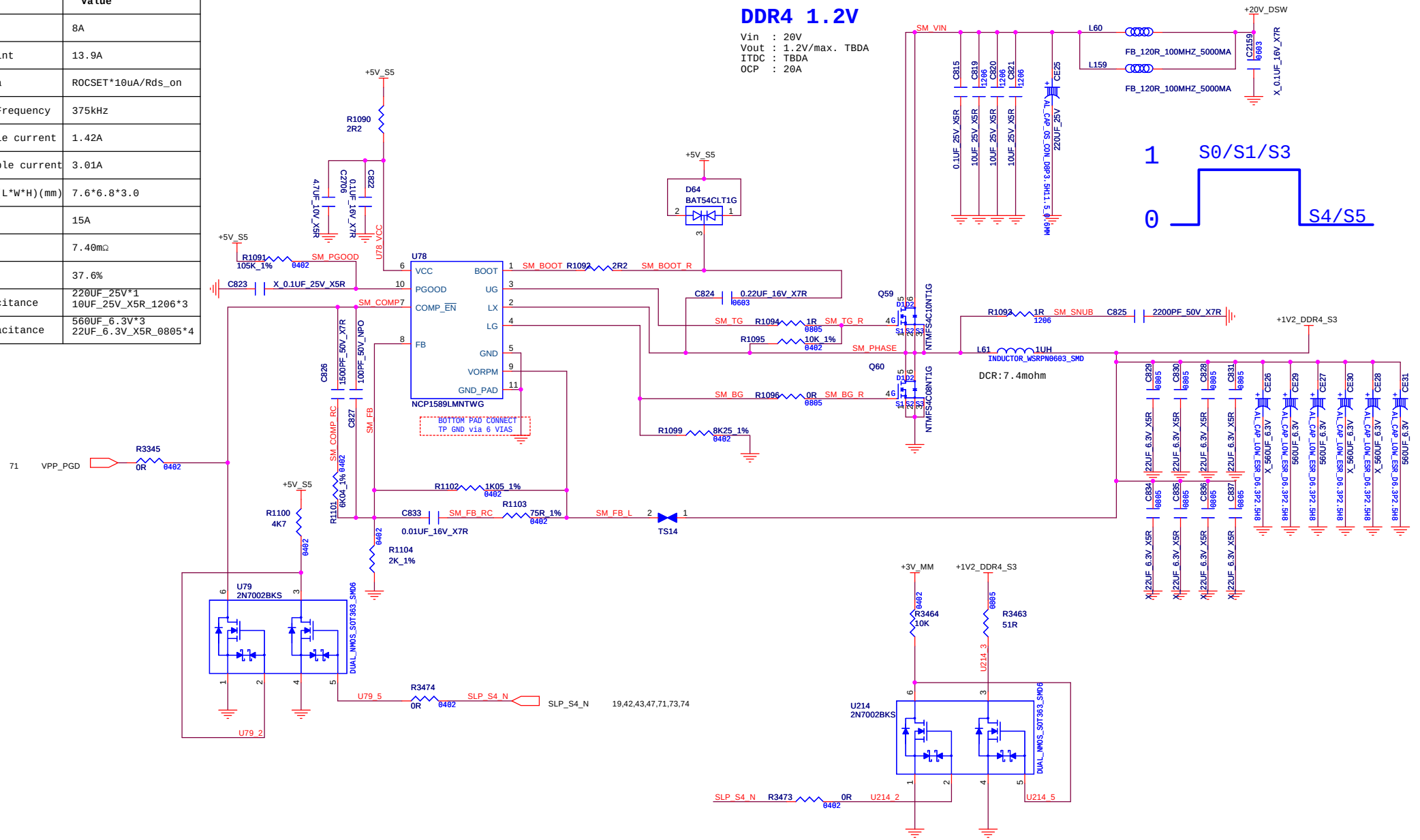
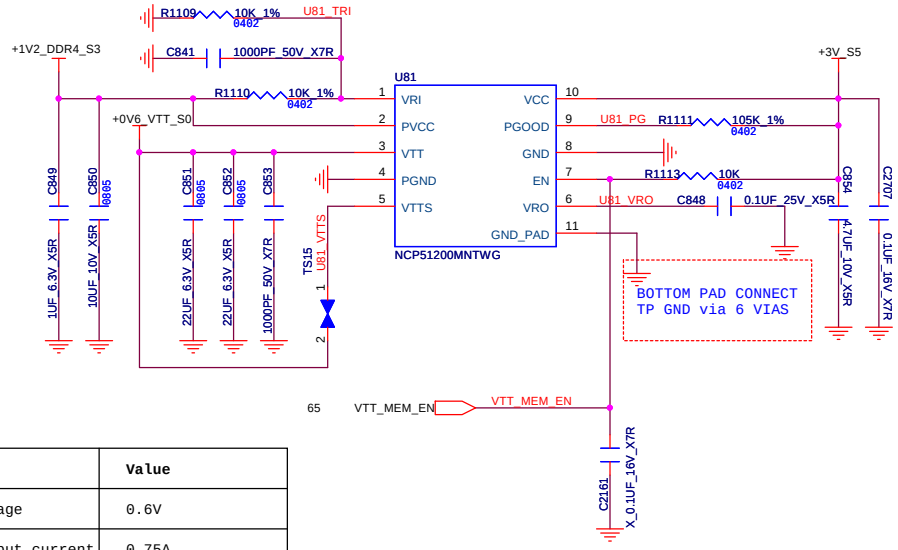
| Parameter | Value |
|---|---|
| Iout.max | 8A |
| OCP set point | 13.9A |
| OCP formula | ROCSET*10uA/Rds_on |
| Switching Frequency | 375kHz |
| Input ripple current | 1.42A |
| Output ripple current | 3.01A |
| Choke_size(L*W*H)(mm) | 7.6*6.8*3.0 |
| Choke_Isat | 15A |
| Choke_DCR | 7.40mΩ |
| Choke_LIR | 37.6% |
| Input capacitance | 220UF_25V*1<br>10UF_25V_X5R_1206*3 |
| Output capacitance | 560UF_6.3V*3<br>22UF_6.3V_X5R_0805*4 |



# 0.6V DDRVTT

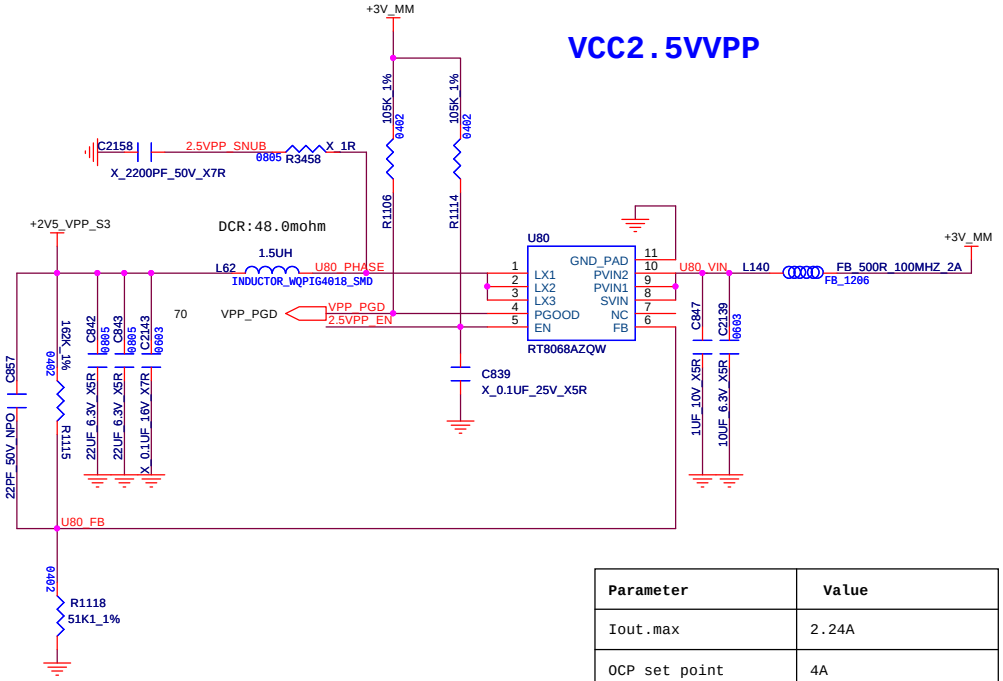
Vin : 1.2V
Vout : 0.6V/ max.0.75A
ITDC :TBDA

S0/S1
1
0
S3/S4/S5

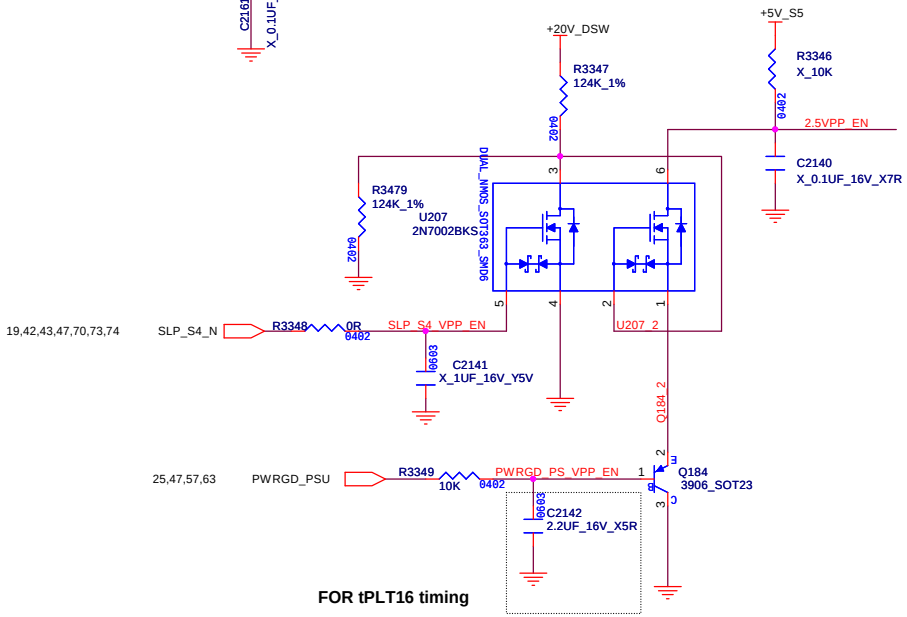



| Parameter | Value |
|---|---|
| Output voltage | 0.6V |
| Maximum output current | 0.75A |
| IC current limit | 4.5A |
| Max. PD(theoretically) | 0.45W |
| Rja | 52.63 °C/W |
| Enable condition | "+3V_S5" ON |

# VCC2.5VPP




| Parameter | Value |
|---|---|
| Iout.max | 2.24A |
| OCP set point | 4A |
| OCP formula | IC controlled |
| Switching Frequency | 1MHz |
| Input ripple current | 0.72A |
| Output ripple current | 0.40A |
| Choke_size(L*W*H)(mm) | 4.3*4.3*2.1 |
| Choke_Isat | 3.3A |
| Choke_DCR | 48.00mΩ |
| Choke_LIR | 22.5% |
| Input capacitance | 10UF_6.3V_X5R_0603*1 |
| Output capacitance | 22UF_6.3V_X5R_0805*2 |




| | |
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| TITLE: M910z VCC2.5V_VPP | REV: V1.0 |
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| Prepared by : KERRY HUANG | |
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| Enable | Disable |
|---|---|
| EN1,EN2 > 1.4 V | EN1,EN2 < 0.4 V |

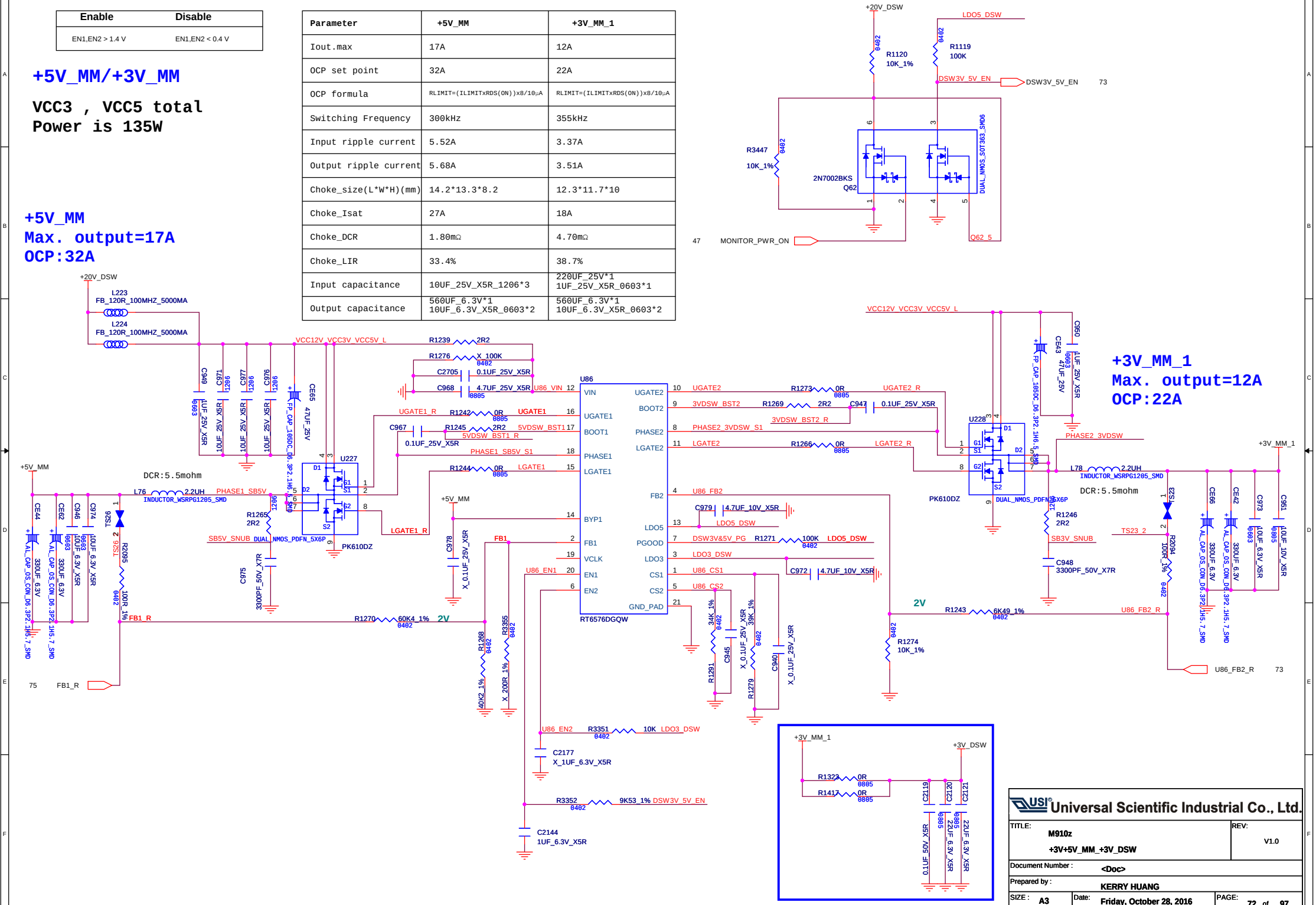
# +5V_MM/+3V_MM

**VCC3 , VCC5 total**
**Power is 135W**

| Parameter | +5V_MM | +3V_MM_1 |
|---|---|---|
| Iout.max | 17A | 12A |
| OCP set point | 32A | 22A |
| OCP formula | RLIMIT=(ILIMITxRDS(ON))x8/10μA | RLIMIT=(ILIMITxRDS(ON))x8/10μA |
| Switching Frequency | 300kHz | 355kHz |
| Input ripple current | 5.52A | 3.37A |
| Output ripple current | 5.68A | 3.51A |
| Choke_size(L*W*H)(mm) | 14.2*13.3*8.2 | 12.3*11.7*10 |
| Choke_Isat | 27A | 18A |
| Choke_DCR | 1.80mΩ | 4.70mΩ |
| Choke_LIR | 33.4% | 38.7% |
| Input capacitance | 10UF_25V_X5R_1206*3 | 220UF_25V*1<br>1UF_25V_X5R_0603*1 |
| Output capacitance | 560UF_6.3V*1<br>10UF_6.3V_X5R_0603*2 | 560UF_6.3V*1<br>10UF_6.3V_X5R_0603*2 |

## +5V_MM
**Max. output=17A**
**OCP:32A**

## +3V_MM_1
**Max. output=12A**
**OCP:22A**




| | |
|---|---|
| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M910z<br>+3V+5V_MM_+3V_DSW | REV: V1.0 |
| Document Number : <Doc> | |
| Prepared by : KERRY HUANG | |
| SIZE : A3 | Date: Friday, October 28, 2016 |
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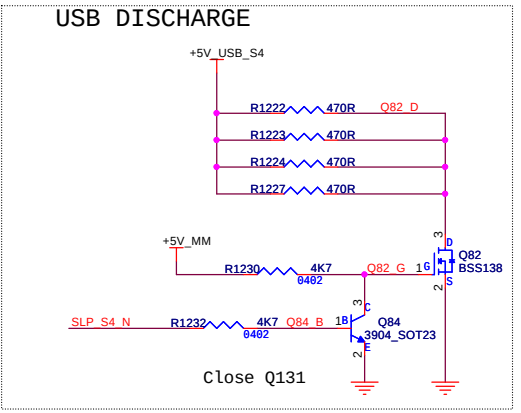
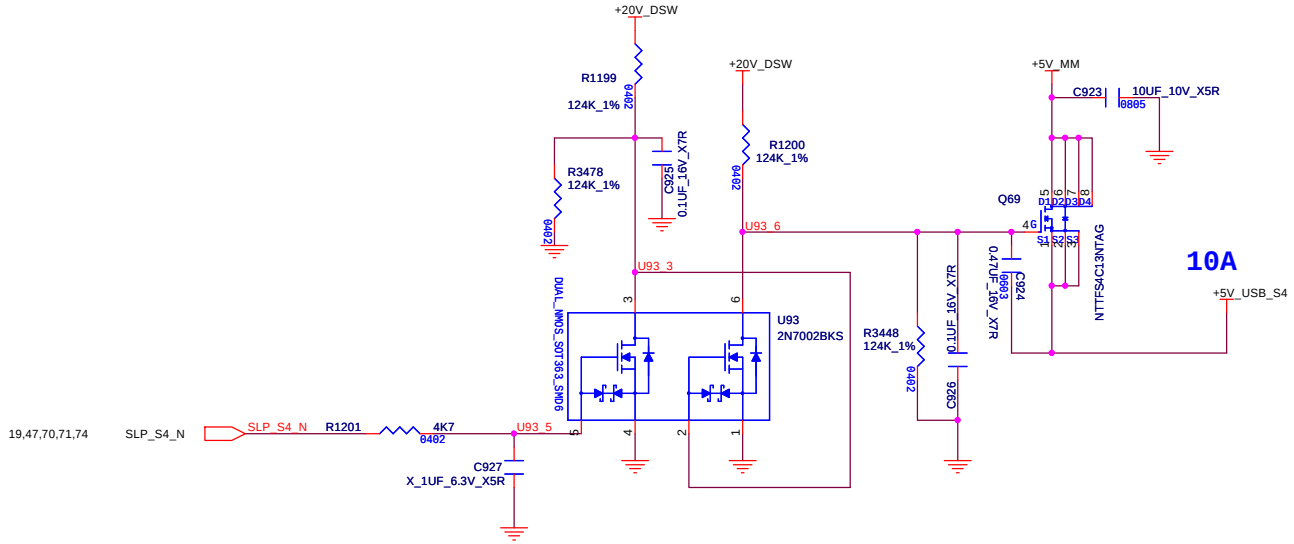
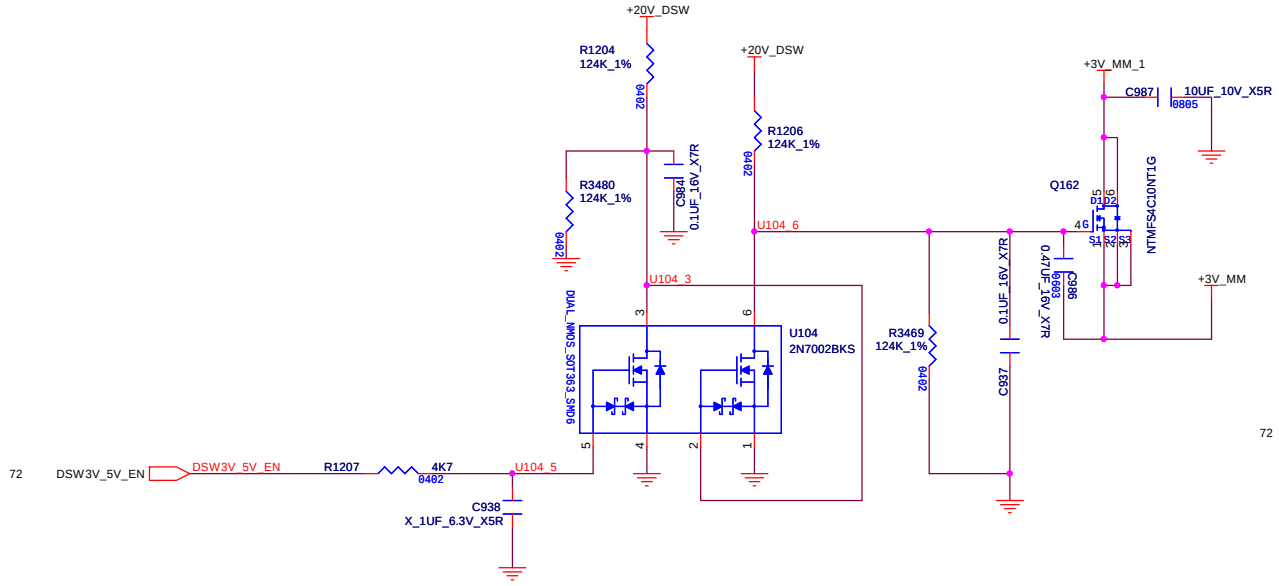
# 5V_USB

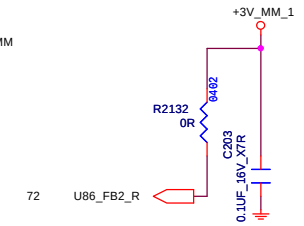
S0~S3 = 1

S4~S5 = 0



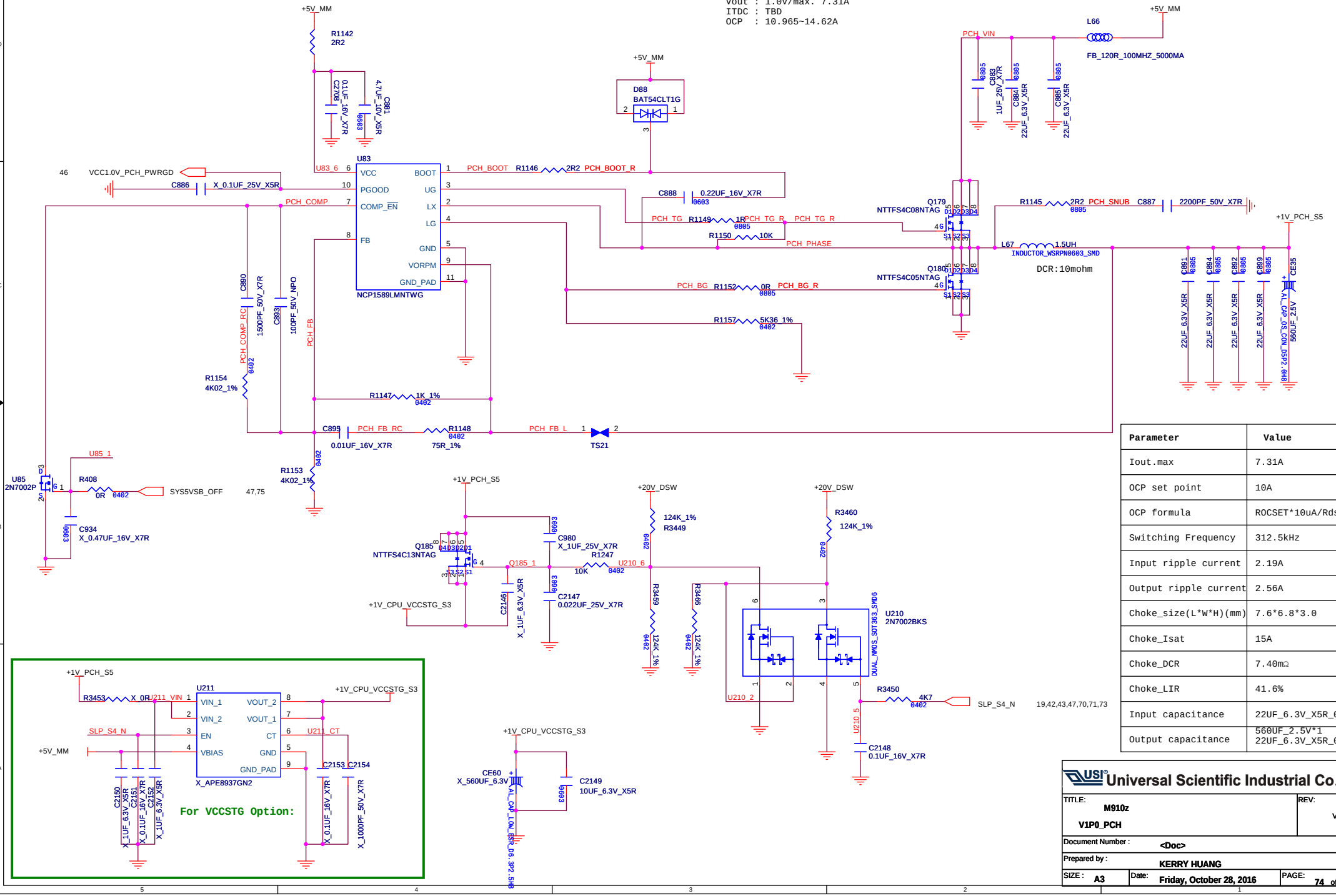




| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z 5V_USB VR | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 73 of 97 | |

# +1V_PCH_S5

Vin : 5V
Vout : 1.0V/max. 7.31A
ITDC : TBD
OCP : 10.965~14.62A




| Parameter | Value |
|---|---|
| Iout.max | 7.31A |
| OCP set point | 10A |
| OCP formula | ROCSET*10uA/Rds_on |
| Switching Frequency | 312.5kHz |
| Input ripple current | 2.19A |
| Output ripple current | 2.56A |
| Choke_size(L*W*H)(mm) | 7.6*6.8*3.0 |
| Choke_Isat | 15A |
| Choke_DCR | 7.40mΩ |
| Choke_LIR | 41.6% |
| Input capacitance | 22UF_6.3V_X5R_0805*2 |
| Output capacitance | 560UF_2.5V*1<br>22UF_6.3V_X5R_0805*4 |

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| | | |
|---|---|---|
| TITLE: M910z<br>V1P0_PCH | | REV: V1.0 |
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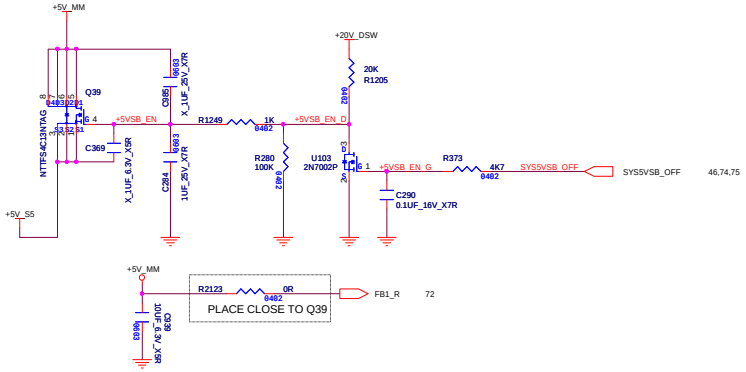
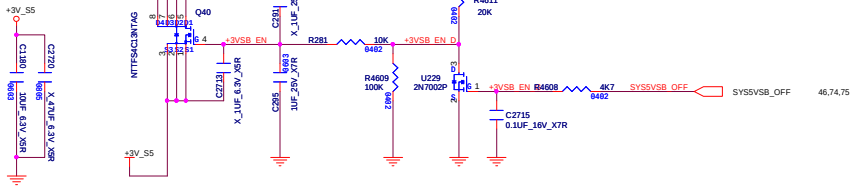
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 74 of 97 |

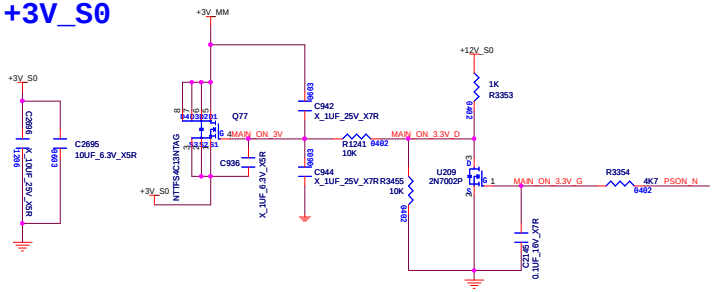
# STAND BY POWER CONTROL



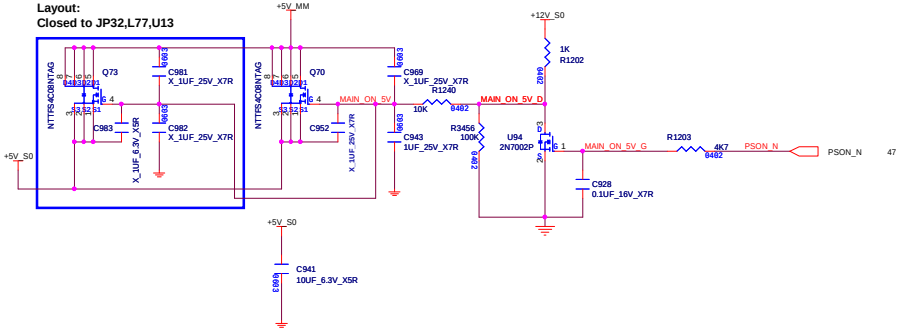




# SYSTEM POWER CONTROL

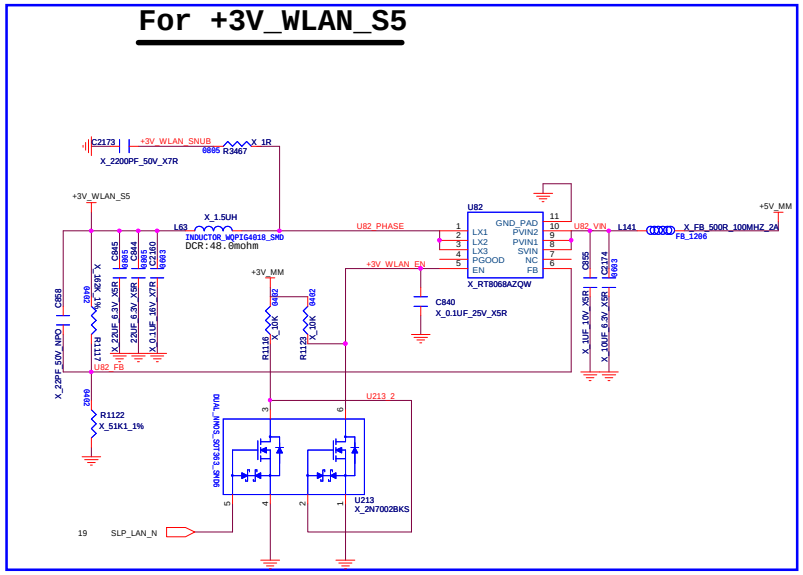
## +3V_S0

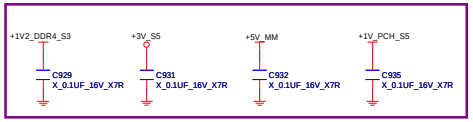



## +5V_S0




## For +3V_WLAN_S5




For EMC

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| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z VCC3/5V | | REV: V1.0 | |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A2 | Date: Friday, October 28, 2016 | PAGE: 75 of 97 | |

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| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z BLANK | | | REV: V1.0 |
| Document Number : | Lenovo_Memphis-Q87 | | |
| Prepared by : | KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 76 of 97 |

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| USB3 # 1 (Capable of OTG) | USB3 # 2 | USB3 # 3 | USB3 # 4 | USB3 # 5 | USB3 # 6 | USB3 # 7 | USB3 # 8 | USB3 # 9 | USB3 #10 | PCIe #5 | PCIe #6 | PCIe #7 | PCIe #8 | PCIe #9 | PCIe #10 | PCIe #11 | PCIe #12 | PCIe #13 | PCIe #14 | PCIe #15 | PCIe #16 | PCIe #17 | PCIe #18 | PCIe #19 | PCIe #20 |
| | SSIC # 1 | SSIC # 2 | | | | PCIe #1 | PCIe #2 | PCIe #3 | PCIe #4 | GbE | | | | SATA #0 | SATA #1 | | GbE | SATA #0 | SATA #1 | SATA #2 | SATA #3 | SATA #4 | SATA #5 | | |
| | | | | | | | | | GbE | | | | | GbE | | | | GbE | | | | | | | |
| | | | | | | X4 | | | | X4 | | | | X4 | | | | X4 | | | | X4 | | | |
| | | | | | | X2 | | X2 | | X2 | | X2 | | X2 | | X2 | | X2 | | X2 | | X2 | | X2 | |
| | | | | | | No Remapping | | | | | | | | Intel PCIe Storage Device #1 | | | | | | | | Intel PCIe Storage Device #2 | | | |

| 27 | 28 | 29 | 30 |
|---|---|---|---|
| PCIe #21 | PCIe #22 | PCIe #23 | PCIe #24 |
| X4 | | | |
| X2 | | X2 | |
| Intel PCIe Storage Device #3 | | | |

# Flexible IO Assign

***B250: ONLY FLEX. IO 27~30 SUPPORT Optane**

| | | |
|---|---|---|
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| TITLE: M910z Flexible IO | | REV: V1.0 |
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| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 77 of 97 |

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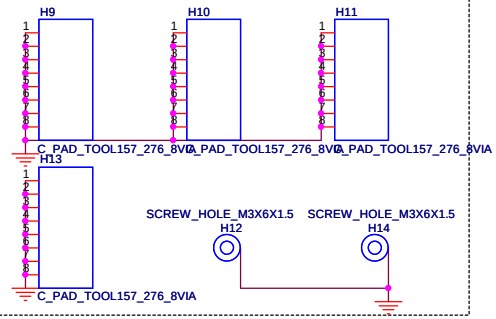
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z BLANK | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 78 of 97 |

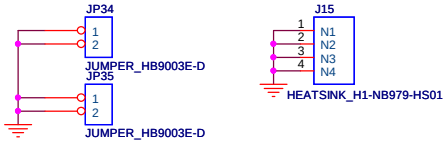
## HEAT PIPE SCREW HOLES



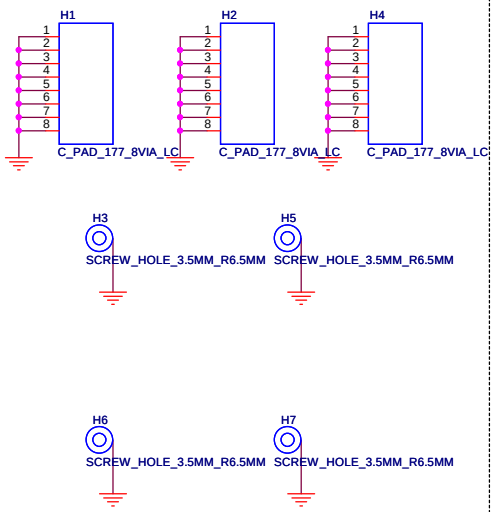

## CPU SOCKET

10/22 MODIFY (LENOVO)

## PCH HEAT SINK




## SCREW HOLES

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| | | |
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| TITLE: M910z HOLE_HEATSINK | | REV: V1.0 |
| Document Number : <Doc> | | |
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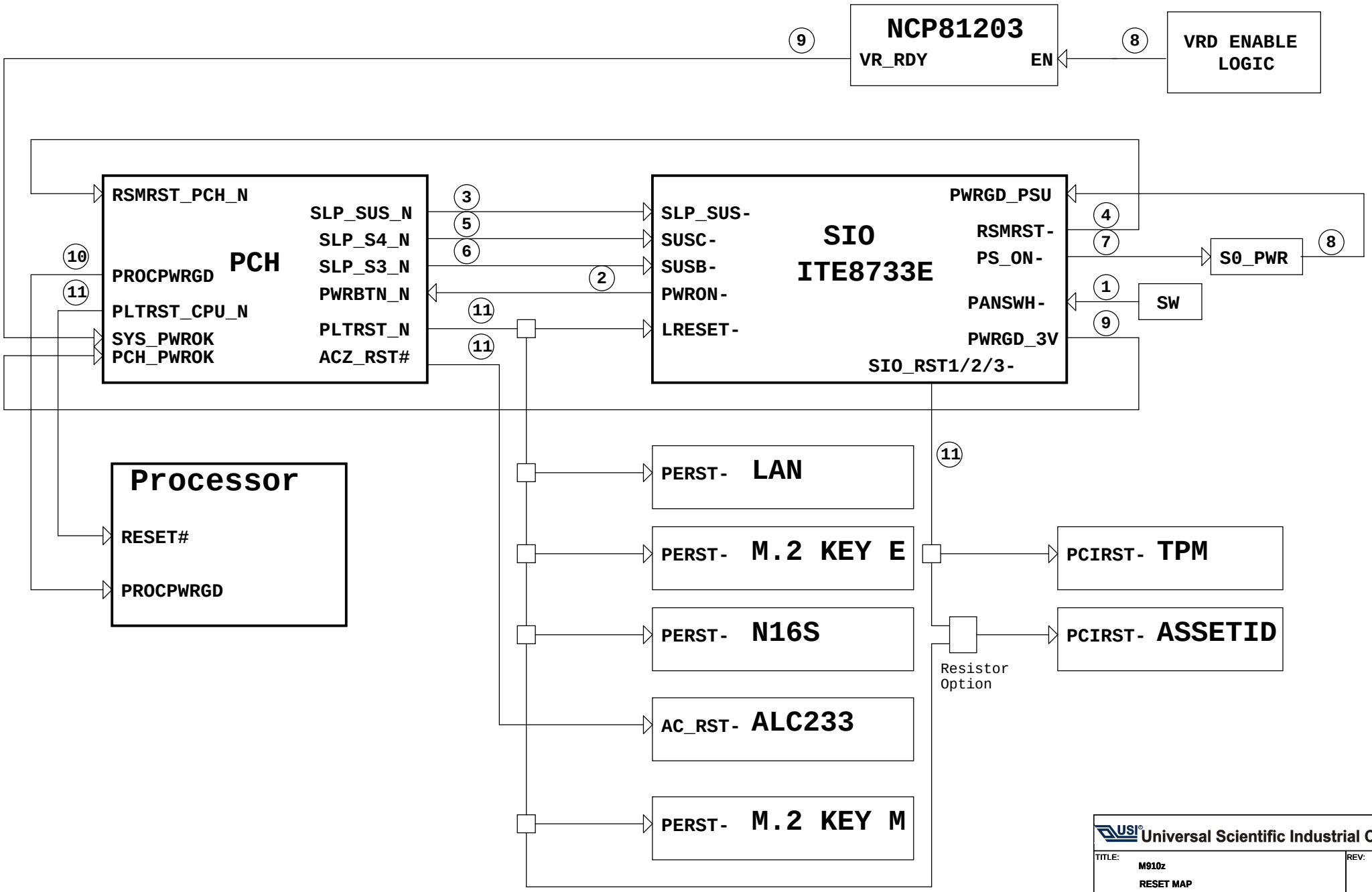
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 79 of 97 |

# RESET MAP

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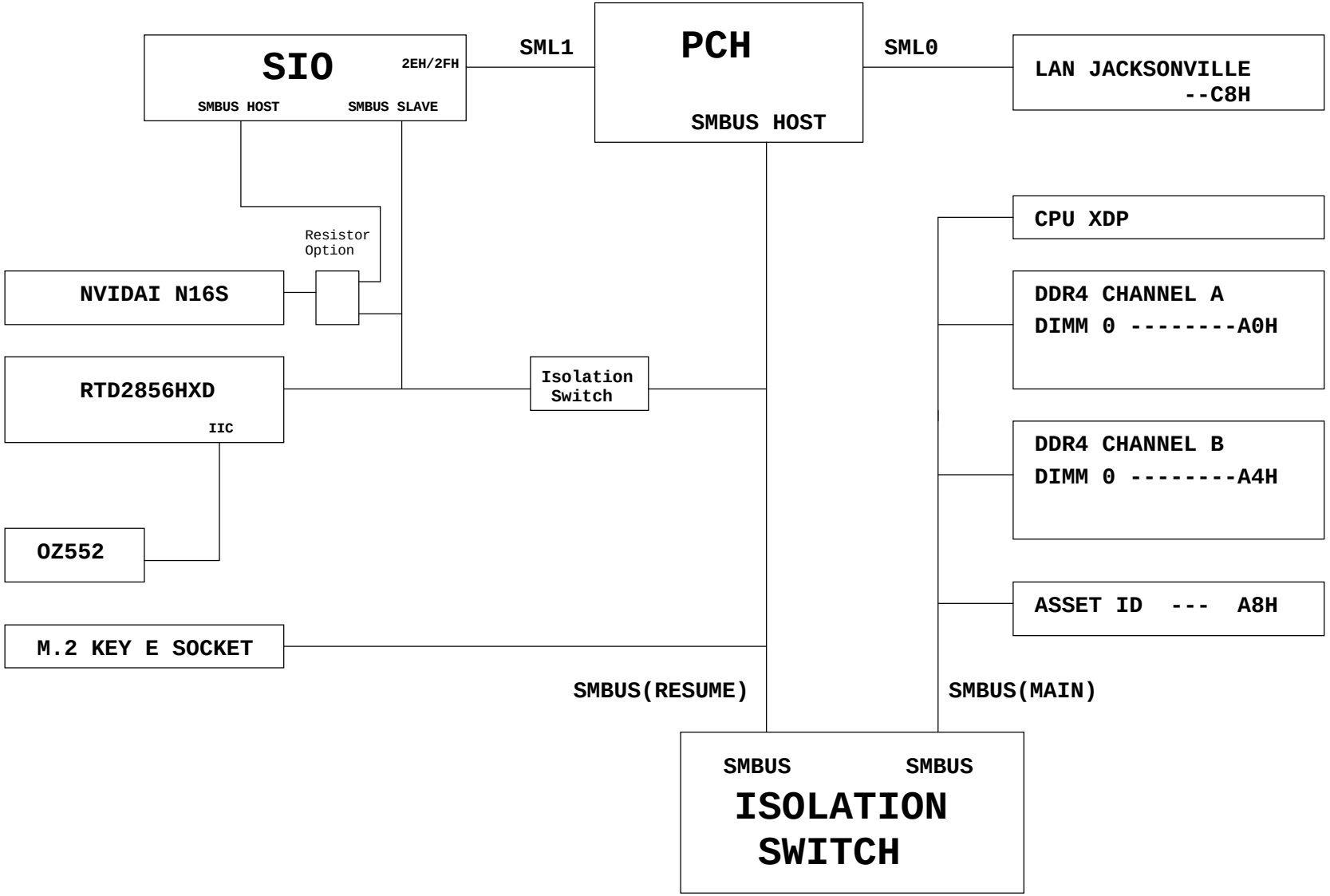
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z RESET MAP | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 80 of 97 |

# SMBUS MAP

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| TITLE: M910z SMBUS MAP | | REV: V1.0 |
| Document Number : <Doc> | | |
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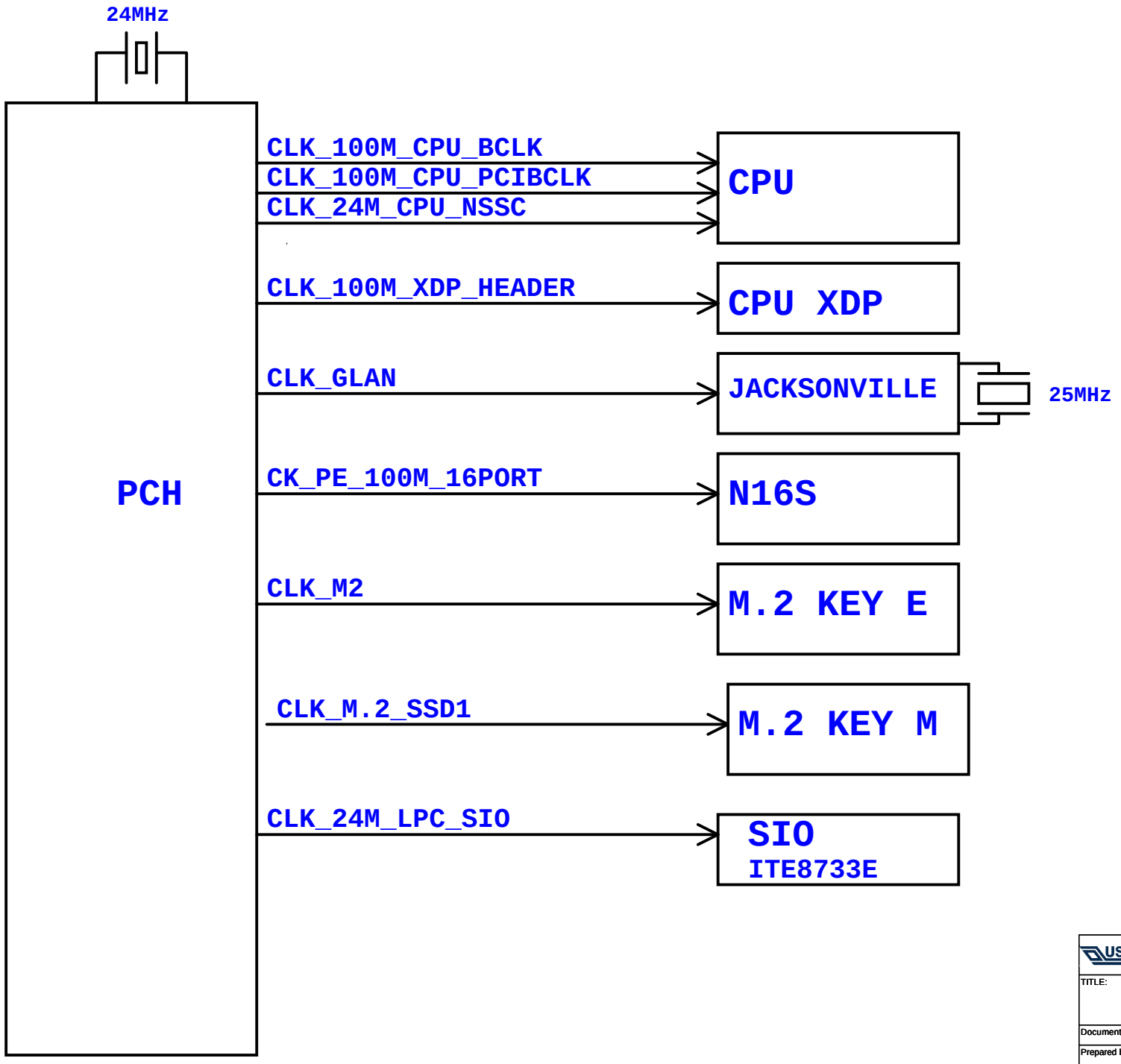
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 81 of 97 |

# CLOCKS DIAGRAM

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| TITLE: M910z CLOCK DISTRIBUTION | | REV: V1.0 |
| Document Number : <Doc> | | |
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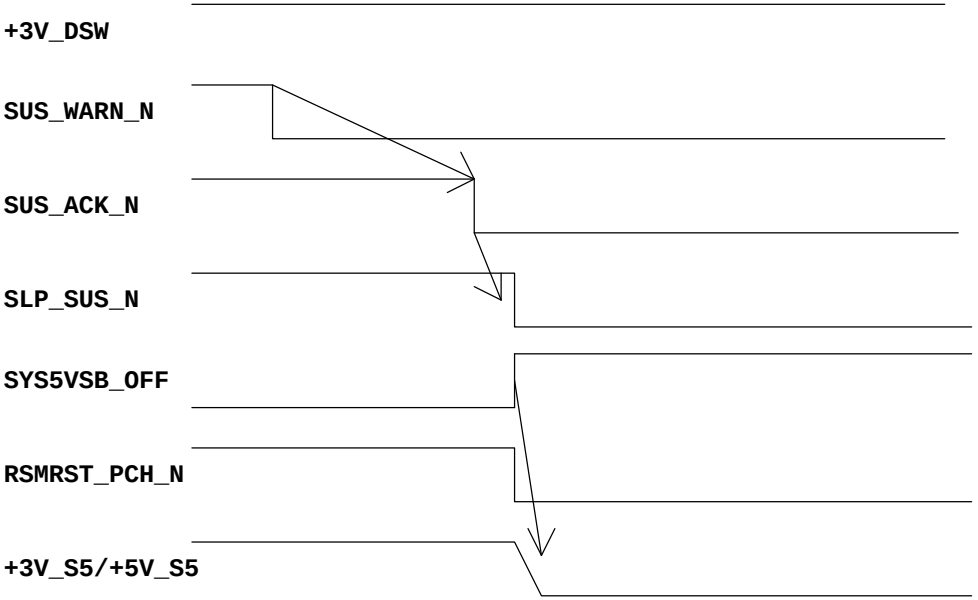
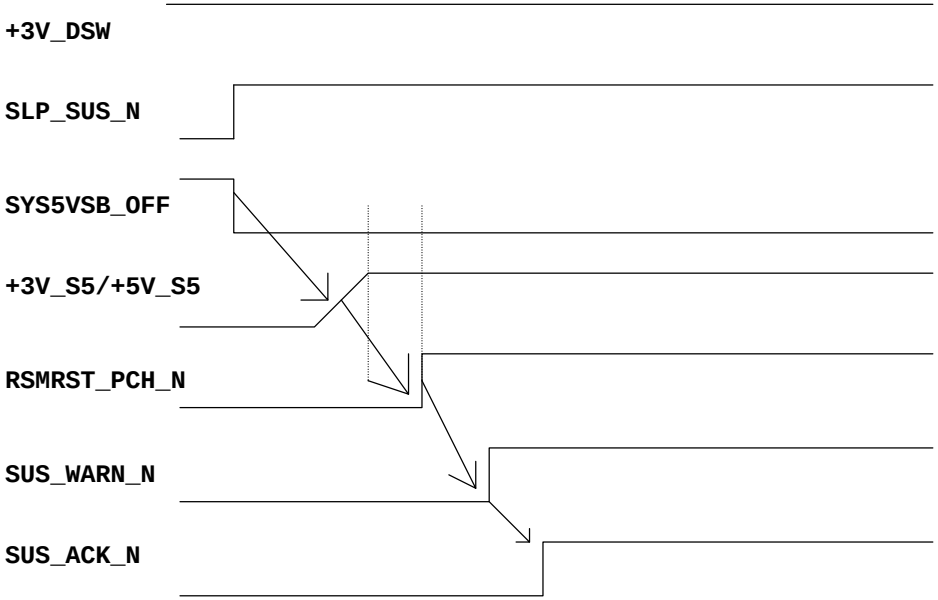
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 82 of 97 |

# Enter DSW State timing diagram




# Exit DSW State timing diagram

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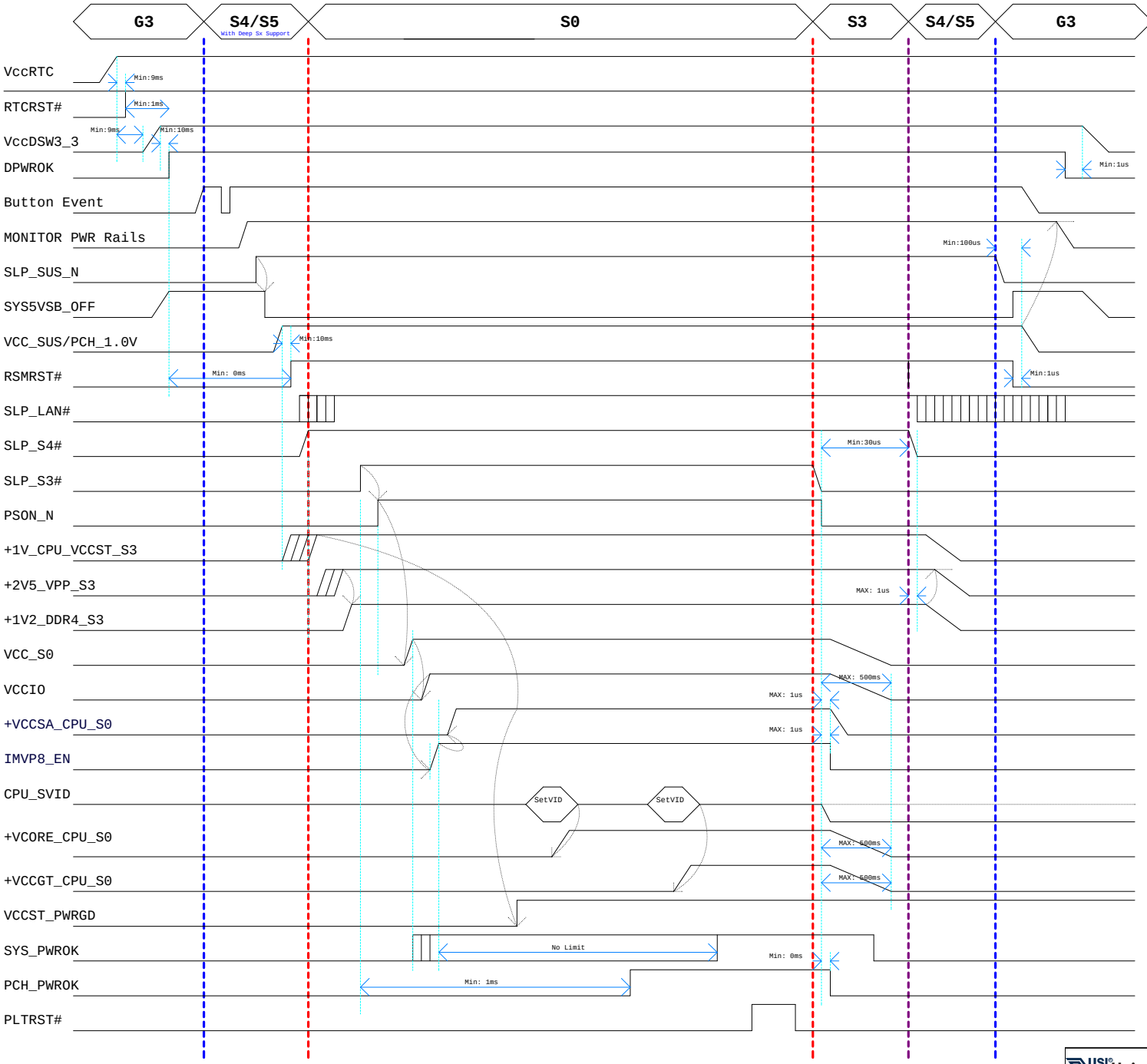
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z DSW SEQUENCING | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 83 of 97 |

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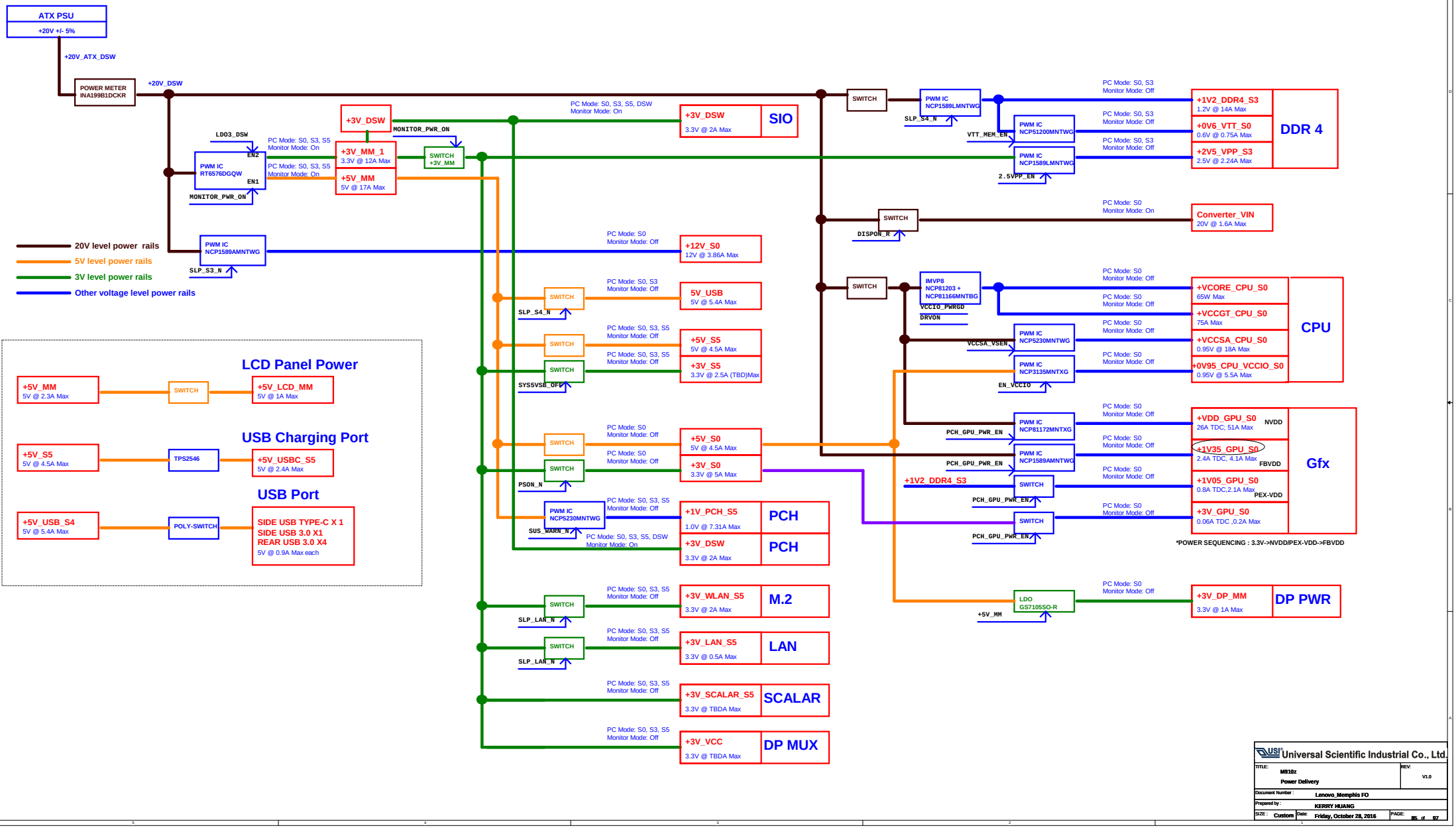
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z POWER SEQUENCING | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : Custom | Date: Friday, October 28, 2016 | | PAGE: 84 of 97 |

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| Universal Scientific Industrial Co., Ltd. | |
| TITLE: M810z Power Delivery | REV: V1.0 |
| Document Number : Lenovo_Memphis FO | |
| Prepared by : KERRY HUANG | |
| SIZE : Custom | Date: Friday, October 28, 2016 |
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| | | |
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z<br>KBL-PCH GPIO Table 1 | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 86 of 97 |

| | | |
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z<br>KBL-PCH GPIO Table 2 | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 87 of 97 |

| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z<br>KBL-PCH GPIO Table 3 | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 88 of 97 |

| | | |
|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | |
| TITLE: M910z<br>KBL-PCH GPIO Table 4 | | REV: V1.0 |
| Document Number : <Doc> | | |
| Prepared by : KERRY HUANG | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 89 of 97 |

| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z<br>KBL-PCH GPIO Table 5 | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 90 of 97 |

| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z<br>KBL-PCH GPIO Table 6 | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 91 of 97 |

| Signal | Usage | When Sampled | Internal PU/PD | Definition | | M900z Setting |
|---|---|---|---|---|---|---|
| | | | | Set To | Description | |
| SPKR / GPP_B14 | Top Swap Override | Rising edge of PCH_PWROK | Weak PD | 0 | Disable "Top Swap" mode (Default) | 0 (No external PD) |
| | | | | 1 | Enable "Top Swap" mode | |
| GSPI0_MOSI / GPP_B18 | No Reboot | Rising edge of PCH_PWROK | Weak PD | 0 | Disable "No Reboot" mode | 0 (PD R116 1K) |
| | | | | 1 | Enable "No Reboot" mode | |
| SMBALERT# / GPP_C2 | TLS Confidentiality | Rising edge of RSMRST# | Weak PD | 0 | Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality) | 1 (PU R499 4K7) |
| | | | | 1 | Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality) | |
| GSPI1_MOSI / GPP_B22 | Boot BIOS Strap Bit BBS | Rising edge of PCH_PWROK | Weak PD | 0 | SPI | 0 (No external PD) |
| | | | | 1 | LPC | |
| SML0ALERT# / GPP_C5 | eSPI or LPC | Rising edge of RSMRST# | Weak PD | 0 | LPC Is selected for EC | 0 (No external PD) |
| | | | | 1 | eSPI Is selected for EC | |
| HDA_SDO | Flash Descriptor Security Override | Rising edge of PCH_PWROK | Weak PD | 0 | Enable security measures defined in the Flash Descriptor | 0 (No external PD) |
| | | | | 1 | Disable Flash Descriptor Security (override) | |
| DDPB_CTRLDATA / GPP_I6 | Display Port B Detected | Rising edge of PCH_PWROK | Weak PD | 0 | Port B is not detected | 0 (No external PD) |
| | | | | 1 | Port B is detected | |
| DDPC_CTRLDATA / GPP_I8 | Display Port C Detected | Rising edge of PCH_PWROK | Weak PD | 0 | Port C is not detected | 0 (No external PD) |
| | | | | 1 | Port C is detected | |
| DDPD_CTRLDATA / GPP_I10 | Display Port D Detected | Rising edge of PCH_PWROK | Weak PD | 0 | Port D is not detected | 0 (No external PD) |
| | | | | 1 | Port D is detected | |

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| | | |
|---|---|---|
| TITLE: M910z KBL-PCH Strapping | | REV: V1.0 |
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| SIZE : A4 | Date: Friday, October 28, 2016 | PAGE: 92 of 97 |

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|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z<br>SIO GPIO Table 1 | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | | PAGE: 93 of 97 |

# COMPRESSED IMAGE

| | | | |
|---|---|---|---|
| Universal Scientific Industrial Co., Ltd. | | | |
| TITLE: M910z SIO GPIO Table 2 | | | REV: V1.0 |
| Document Number : <Doc> | | | |
| Prepared by : KERRY HUANG | | | |
| SIZE : A3 | Date: Friday, October 28, 2016 | PAGE: 94 of 97 | |

## RTD2586HXD SCALER GPIO TABLE

| PIN | Signal Name | Description | Voltage | IN/OUT | M900 Usage |
|---|---|---|---|---|---|
| 64 | P1.0/T2(I) /INT1(I) | GPIO /PWM0 /PWM3 /SD0 /SPDIF0 | 5V tolerance even when power-off | OUT | LCD_BKLTEN |
| 65 | P1.1/T2EX(I) | GPIO /PWM1 /WS | 5V tolerance even when power-off | -- | (No Use) |
| 66 | P1.2/CLKO2(O) | GPIO /SCK | 5V tolerance even when power-off | -- | (No Use) |
| 67 | P1.3 | GPIO /MCK | 5V tolerance even when power-off | -- | (No Use) |
| 68 | P1.4 | GPIO /SD0 /SPDIF | 5V tolerance even when power-off | -- | (No Use) |
| 69 | P1.5 | GPIO /SD1 /SPDIF1 /IICSCL | 5V tolerance even when power-off | -- | (No Use) |
| 70 | P1.6 | GPIO /SD2 /SPDIF2 /IICSDA | 5V tolerance even when power-off | -- | (No Use) |
| 71 | P1.7 | GPIO /PWM1 /PWM5 /SD3 /SPDIF3 | 5V tolerance even when power-off | -- | (No Use) |
| 58 | P3.0/RXD(I/O) | DDCSCL1 /GPIO | 5V tolerance even when power-off | IN/OUT | RTLD2586_SMBCLK |
| 59 | P3.1/TXD(O) | DDCSDA1 /GPIO | 5V tolerance even when power-off | IN/OUT | RTLD2586_SMBDATA |
| 109 | P3.2/INT0(I) | GPIO /PWM2 /SCK /AUX_D1 | 5V tolerance even when power-off | -- | (No Use) |
| 110 | P3.3/INT1(I) | GPIO /WS /SD1 | 5V tolerance even when power-off | -- | (No Use) |
| 111 | P3.4/T0 | GPIO /SD0 /SPDIF0 | 5V tolerance even when power-off | IN | MUX_HPD |
| 112 | P3.5(BS)/T1 | GPIO /SD1 /WS /SPDIF1 | 5V tolerance even when power-off | IN | DP_SOURCE_HPD |
| 114 | P3.7 | GPIO /PWM4 /SD3 /MCK /SPDIF3 | 5V tolerance even when power-off | -- | (No Use) |
| 96 | P5.2 | GPIO /PWM0 | 5V tolerance | -- | (No Use) |
| 97 | P5.3 | GPIO /PWM1 | 5V tolerance | -- | (No Use) |
| 98 | P5.4 | GPIO /PWM2 | 5V tolerance | -- | (No Use) |
| 99 | P5.5 | GPIO /PWM3 | 5V tolerance | -- | (No Use) |
| 100 | P5.6 | GPIO /PWM4 | 5V tolerance even when power-off | -- | (No Use) |
| 101 | P5.7 | GPIO /PWM5 | 5V tolerance even when power-off | -- | (No Use) |
| 50 | P6.0 | A-ADC0 /GPIO | 5V tolerance | -- | (No Use) |
| 51 | P6.1 | A-ADC1 /GPIO | 5V tolerance | -- | (No Use) |
| 52 | P6.2 | A-ADC2 /GPIO /USB_DDCSCL1 | 5V tolerance | -- | (No Use) |
| 53 | P6.3 | ADC3 /GPIO /USB_DDCSDA1 | 5V tolerance | -- | (No Use) |
| 54 | P6.4 | GPIO /PWM4 | 5V tolerance even when power-off | OUT | PANEL_ON |
| 55 | P6.5 | GPIO_USB /PWM1 /PWM5 | 5V tolerance even when power-off | OUT | SYSTEM_EEPROM_WP |
| 56 | P6.6 | GPIO /IICSCL | 5V tolerance even when power-off | Native | EESCL |
| 57 | P6.7 | GPIO /IICSDA | 5V tolerance even when power-off | Native | EESDA |
| 124 | P7.0 | DDCSCL2 /GPIO /AUX_CH_P0 | 5V tolerance even when power-off | Native | MUX_AUXP |
| 123 | P7.1 | DDCSDA2 /GPIO /AUX_CH_N0 | 5V tolerance even when power-off | Native | MUX_AUXN |
| 122 | P7.2 | DDCSDA3 /GPIO /AUX_CH_N1 | 5V tolerance even when power-off | Native | DPIN_AUXN |


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TITLE: M910z
SIO GPIO Table 3

REV: V1.0

Document Number : <Doc>

Prepared by : KERRY HUANG

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| | | | | | |
|---|---|---|---|---|---|
| 121 | P7.3 | DDCSCL3 /GPIO /AUX_CH_P1 | 5V tolerance even when power-off | Native | DPIN_AUXP |
| 104 | P7.4 | GPIO /SD1 /SPDIF1 /IRQB /IICSDA / | 5V tolerance even when power-off | Native | PANEL_SMBUS_DATA |
| 103 | P7.5 | GPIO /PWM1 /SD2 /SPDIF2 /IICSCL | 5V tolerance even when power-off (GPIO OD) | Native | PANEL_SMBUS_CLK |
| 102 | P7.6 | GPIO /PWM0 /SD3 /SPDIF3 | 5V tolerance even when power-off | -- | (No Use) |
| 105 | P8.0 | GPIO /SD0 /SPDIF0 /AUX_TXDATA | 5V tolerance even when power-off | -- | (No Use) |
| 108 | P8.1/CLKO1(O) | GPIO /MCK /AUX_OE | 5V tolerance even when power-off | Native | FLASH_WP |
| 74 | P9.0 | TXO3+_8b /GPIO /IIS_SD0 /SPDIF0 | 3.3V tolerance | Native | LCD1DO3 |
| 75 | P9.1 | TXO3-_8b /GPIO /IIS_MCK /SPDIF1 | 3.3V tolerance | Native | LCD1DO3# |
| 76 | P9.2 | TXOC+_8b /GPIO | 3.3V tolerance | Native | LCD1CLK |
| 77 | P9.3 | TXOC-_8b /GPIO | 3.3V tolerance | Native | LCD1CLK# |
| 78 | P9.4 | TXO2+_8b /GPIO /IIS_SCK /SPDIF2 | 3.3V tolerance | Native | LCD1DO2 |
| 79 | PA.0 | TXO2-_8b /GPIO /IIS_WS /SPDIF3 | 3.3V tolerance | Native | LCD1DO2# |
| 80 | PA.1 | TXO1+_8b /GPIO | 3.3V tolerance | Native | LCD1DO1 |
| 81 | PA.2 | TXO1-_8b /GPIO | 3.3V tolerance | Native | LCD1DO1# |
| 82 | PA.3 | TXO0+_8b /GPIO | 3.3V tolerance | Native | LCD1DO0 |
| 83 | PA.4 | TXO0-_8b /GPIO | 3.3V tolerance | Native | LCD1DO0# |
| 48 | PB.0 | GPIO /PWM0 /AUDIO_HOUTR | 3.3V tolerance | -- | (No Use) |
| 47 | PB.1 | GPIO /SD0 /AUDIO_HOUTL | 3.3V tolerance | -- | (No Use) |
| 46 | PB.2 | GPIO /MCK /AUDIO_SOUTR | 3.3V tolerance | -- | (No Use) |
| 45 | PB.3 | GPIO /SCK /AUDIO_SOUTL | 3.3V tolerance | -- | (No Use) |
| 44 | PB.4 | GPIO /PWM5 /WS /SPDIF3 /AUDIO_REF | 3.3V tolerance | -- | (No Use) |
| 43 | PB.5 | GPIO /LINE_INR /IICSDA | 3.3V tolerance | -- | (No Use) |
| 42 | PB.6 | GPIO /LINE_INL /IICSCL | 3.3V tolerance | -- | (No Use) |
| 41 | PB.7 | | 5V tolerance even when power-off | IN | PWM_EN_SW |
| 126 | PC.0 | GPIO /PMW0 /PWM1 /SPDIF2 /CEC | 5V tolerance even when power-off | -- | (No Use) |
| 119 | PC.1 | GPO /PWM1 /PWM5 /SPDIF1 (Power on latch Pin .) (when AC Power On , Power on latch Pin must be "High" ) | 5V tolerance even when power-off | -- | PWR_LATCH (STRAP) |
| 72 | PC.2 | GPIO /PWM3 | 5V tolerance even when power-off | -- | (No Use) |
| 63 | PC.3 /INT0(I) | GPIO /PWM2 | 5V tolerance even when power-off | OUT | BKLTCTL_R |
| 40 | PC.4 | | 5V tolerance even when power-off | IN/OUT | MONI_INT |
| 39 | PD.0 | | 5V tolerance even when power-off | OUT | MONI_ACK |
| 37 | PD.1 | | 3.3V tolerance | IN | LCD_ID0 |
| 36 | PD.2 | | 3.3V tolerance | IN | LCD_ID1 |
| 35 | PD.3 | | 3.3V tolerance | IN | LCD_ID2 |
| 34 | PD.4 | | 3.3V tolerance | IN | LCD_ID3 |
| 33 | PD.5 | | 3.3V tolerance | OUT | PWM_EN_SC |
| 32 | PD.6 | | 3.3V tolerance | -- | (No Use) |

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| Document Number : <Doc> | |
| Prepared by : KERRY HUANG | |
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## V0.1 to V0.2 CHAGNE LIST

- ●PAGE18:add R4626 R4627 0R for 24MHZ EMI testing requirment
- ●PAGE21:add R4628 R4629 R4630 R4631 33R for SI fine-tune
- ●PAGE21:nopop R161 10K
- ●PAGE33:exchange SATA port0 and port1 trace routing
- ●PAGE33:pop R422 R426 4K7 and nopop R409 4K7 for SATA RX fine-tune for TI
- ●PAGE33:change U13 re-driver and related R&C from TI to PARADE due to TI TX Gen3 fail.
- ●PAGE34:change M.2 stand-off
- ●PAGE36:add D104 R4615 R3766 C2719 for AMP. de-pop
- ●PAGE37:remove AMP. IC for Lenovo H/W spec. udpate
- ●PAGE39:change JP36 USB TYPE-C connector
- ●PAGE45:change R4546 R4547 R4548 R4549 to 100R for SPI SI fine-tune
- ●PAGE47:change C1202 from 330pF to 680pF to fix PLTRST_N monotonic
- ●PAGE47:nopop C2151 0.1uF to fix SLP_S4 with glitch
- ●PAGE47:nopop R1264 10K
- ●PAGE51:connect N16_CLKREQ_N to PCH and add U230 R4618 R4617 for NV requirement
- ●PAGE51:pop C435 330pF to fix GPU_RST_N monotonic
- ●PAGE57:nopop R735 and use GPU_RST_N to gate SMBUS for NV requirement
- ●PAGE58:change L150 L151 L152 from FB_30R_100MHZ_1000MA to FB_300R_2000MA for NV requirement
- ●PAGE59:add +3V_GPU_S0 and +1V05_GPU_S0 discharge circuit for NV requirement
- ●PAGE60:change R2098 pull high from +3V_S0 to +3V_GPU_S0 for NV requirement
- ●PAGE72:change C731 from 33pF to 100pF for Loadline fine-tuneing
- ●PAGE72:change R1244,R1266 from 2.2R_0805 to 0R_0805 for +5V_MM & +3V_MM_1 driving waveform
- ●PAGE72:change R1279 from 30.9K_1%_0402 to 39K_1%_0402 for +5V_MM OCP fine-tuning
- ●PAGE72:change R1291 from 21.5K_1%_0402 to 34K_1%_0402 for +3V_MM_1 OCP fine-tuning

## V0.2 to V0.3 CHAGNE LIST

- ●PAGE18:change C83 C2649 from 10PF to 15PF for better crystal ppm fine-tune
- ●PAGE19:pop R126 10K to fix deep sleep to S5 on and off continuously issue
- ●PAGE25:nopop JP8 SPI debug header and pop R235 0R for interference issue when plugging M.2 SDD.
- ●PAGE27:change CE43 CE46 CE65 from 56uF to 47uF for popular part
- ●PAGE21:add TS29~TS32 ,R4633 for easy LCD converter measurement.
- ●PAGE30:change C1290 C1291 from 10PF to 18PF for better crystal ppm fine-tune
- ●PAGE30:reserve R4635 R4636 0R for EMI requirement
- ●PAGE31:change R1316 from 10k to 20k to fix LCD power rise time too quick
- ●PAGE33:pop R422 4K7 for better SATA TX jitter
- ●PAGE35:change M.2 SSD power from +3V_S5 to +3V_S0 to fix Erp off mode fail issue
- ●PAGE44:nopop R541 4K7 to fix deep sleep to S5 on and off continuously issue
- ●PAGE47:change R1377 from 1K to 10K to improve Erp.
- ●PAGE45:nopop R4538 and pop R4625 for Erp
- ●PAGE59:nopop C721 1uF for GPU power timing sequencing
- ●PAGE60:change CE46 from 56uF to 47uF for popular part
- ●PAGE60:change R2112 21k_1% to 35k7_1% and Q138 Q142 from NTMFS4C06NT1G to NTMFS4C024N for OCP fine-tune
- ●PAGE61:pop C1333 0.1uF for GPU power timing sequencing
- ●PAGE72:change CE65 from 56uF to 47uF for popular part
- ●PAGE72: change EC51 reservation to C2720 reservation for space saving.

## V0.3 to V0.4 CHAGNE LIST

- ●PAGE03:remove J1 XDP
- ●PAGE16:swap M.2_SSD1_P2 and M.2_SSD1_P3 lane
- ●PAGE19:remove R4572 X_0R to have space to add TP54 for ICT
- ●PAGE39:change R4553 PU +3V_S5 to +3V_SO for realtek FAE requirement.
- ●PAGE45:add R4640 0R and reserve R4641 0R for ST TPM power saving option
- ●PAGE36:add MIC MUTE control circuit ,R4637 R4638 100K_1% ,Q455 2N7002
- ●PAGE47:pop R4579 0R and add R4639 10K for MIC mute funciton
- ●PAGE66:change CE67 from 33UF DIP to 47UF SMD to solve pin shorted issue.

## V0.4 to V1.0 CHAGNE LIST

- ●PAGE30:change R295 R305 PU voltage from +3V_S5 to +3V_SC_VPP_MM to fix +3V_S5 voltage leakage in deep sleep mode when clicking monitor mode button.
- ●PAGE30:add Q457 ,R4644 ,R4645 current blacking circuit to prevent the back drive current in deep sleep mode when clicking monitor mode button.
- ●PAGE30:add R4642 100K PD to avoid floating
- ●PAGE30:add Q456 R4652 R4647 R4643 R4648 to fix +3V_S5 voltage leakage in deep sleep mode when clicking monitor mode button.
- ●PAGE36:remove D104 and add U231 AND gate to avoid +3V_S0 leakage to AUDIO_RST_N
- ●PAGE39:add D102 to fix USB type-C USB2.0 ESD fail.
- ●PAGE46:change R514 from 10K to 100K to increase SYS5VSB_OFF voltage level
- ●PAGE47:nopop R1328 R1329 4K7 to fix +3V_S5 voltage leakage in deep sleep mode
- ●PAGE47:nopop R1377 and pop R1400 to fix +3V_S5 voltage leakage in deep sleep mode when clicking monitor mode button.
- ●PAGE47:nopop R838 and add R4653 to connect VR_HOT to CPU directly for lenovo requirement.

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